AVT6203A
EPD Controller
Hardware Manual

1 Revision History

Version	Comments	Date
V1.0	Initial	Jul.11, 2011
V1.1	Add the REG[164] For RGB Format Select	Jul.29, 2011

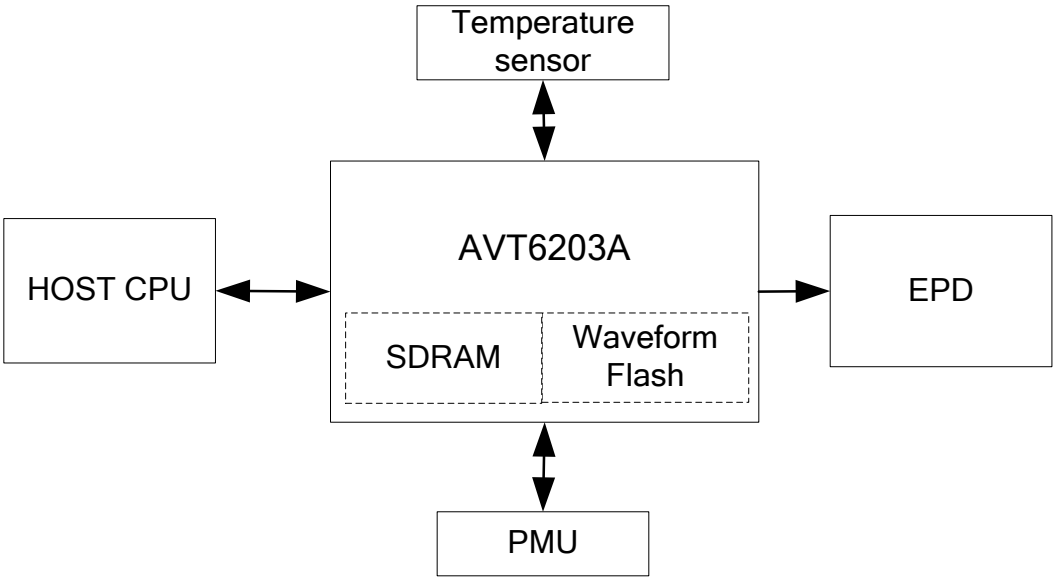
2 Index

3 Introduction

3.1 Summary

AVT6203 EPD controller provides customers a low cost, high efficiency monolithic solution for EPD. The controller can reduce CPU's runtime for displaying and has glueless interface to popular Gate drivers and Source Drivers. It supports 16 regions to update simultaneously and accelerates touch pen, scroll bar and other on-screen user interactive applications. This monolithic solution also provides customized interface for power management unit of the system.

3.2 AVT6203A Reference System



4 Function List

4.1 16-Bits CPU Interface（INTEL80）

- Support 16-Bits I80 interface
- Support register access and SDRAM operation by commands
- Support Packed data and raw data of image transfer

4.2 Source driver and Gate driver Interface

- Glueless interface to AUO, PVI, LG, OED panels
- Configurable timing for source and gate driver

4.3 SDRAM Integration

- Integrate 4Mbyte Mobile SDRAM
- Support 128MHz clock

4.4 Power Control Interface

- Five power control pins with timing configuration for on/off control

4.5 Temperature Sensor Interface

- Support temperature senor of I2C interface, like LM75

4.6 SPI FLASH Interface

- Integrate 4Mbit SPI Flash
- SPI Flash contents: Waveform, Instruction code and Boot setting
- Support high speed Mode

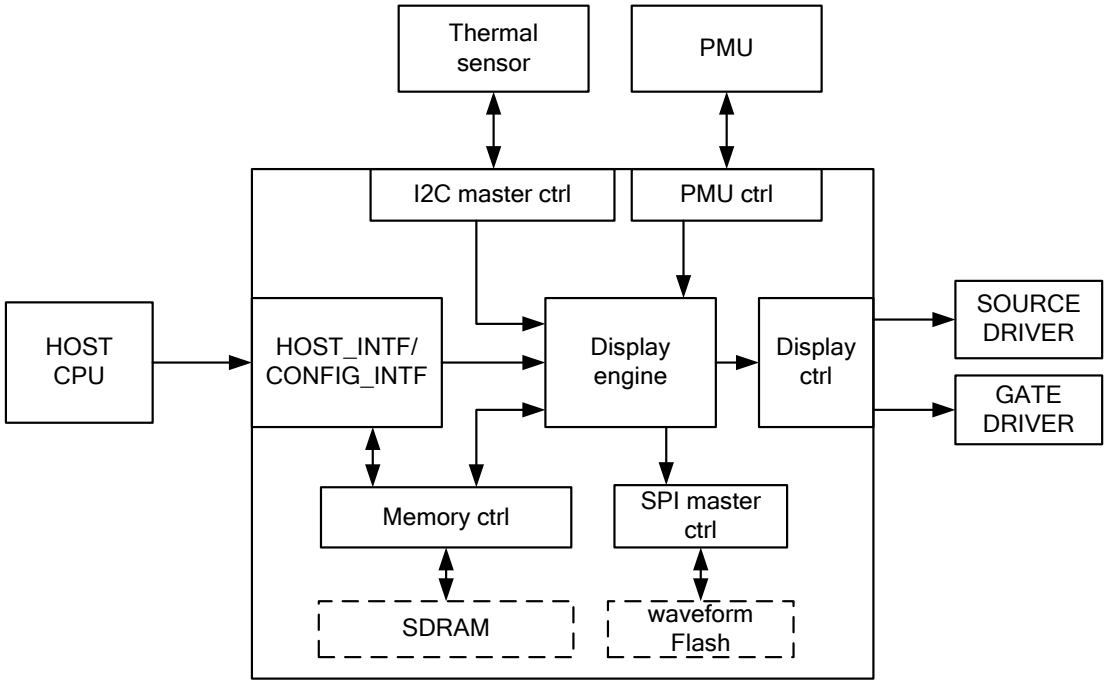
4.7 Clock

- Support CLKI and oscillator for clock input
- Configurable clock frequency by on chip PLL

4.8 Display Function

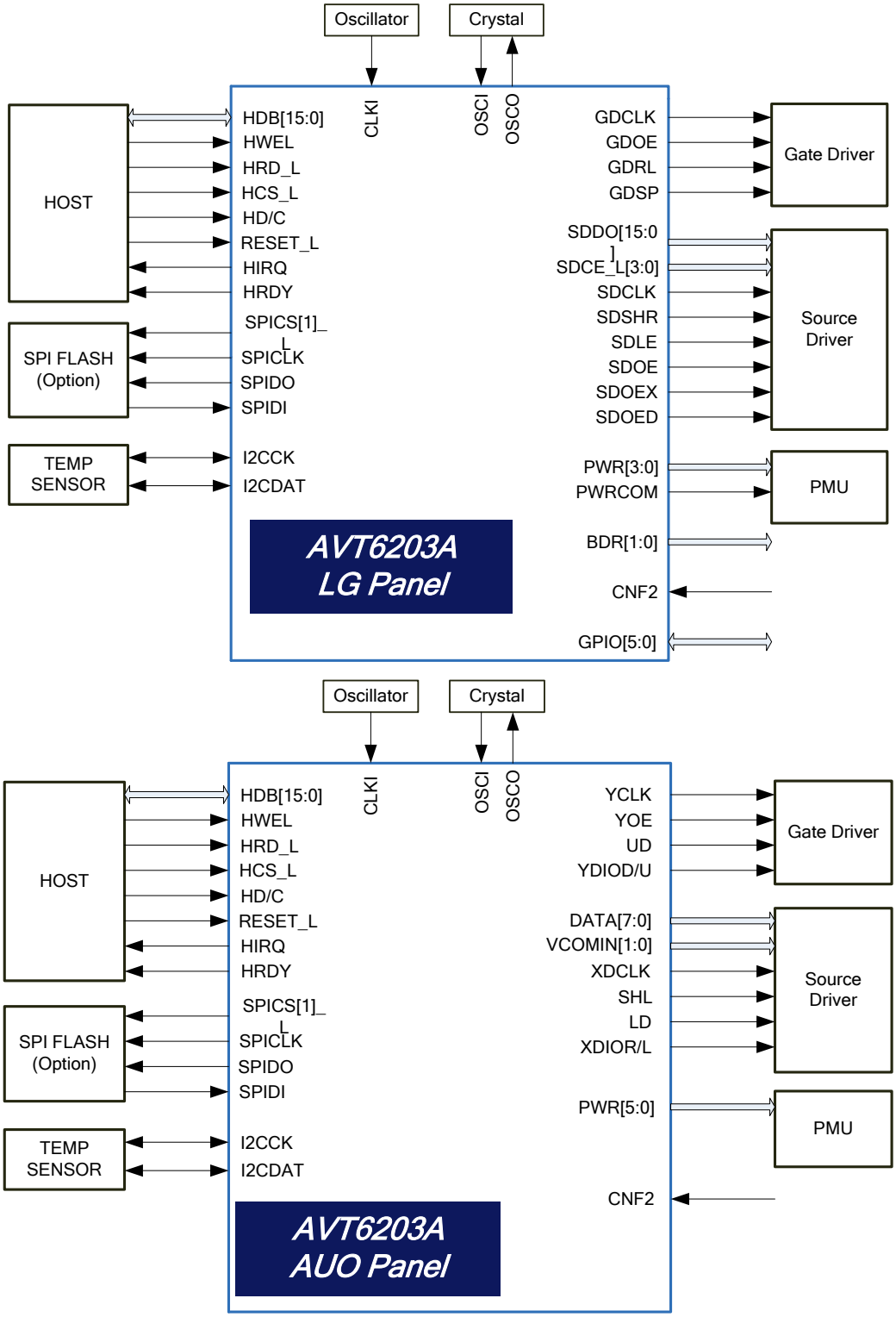
- Support full image and part image update
- Support 15 waveform modes
- Support 16 LUT pipeline update
- Support image rotation

5 Function Description



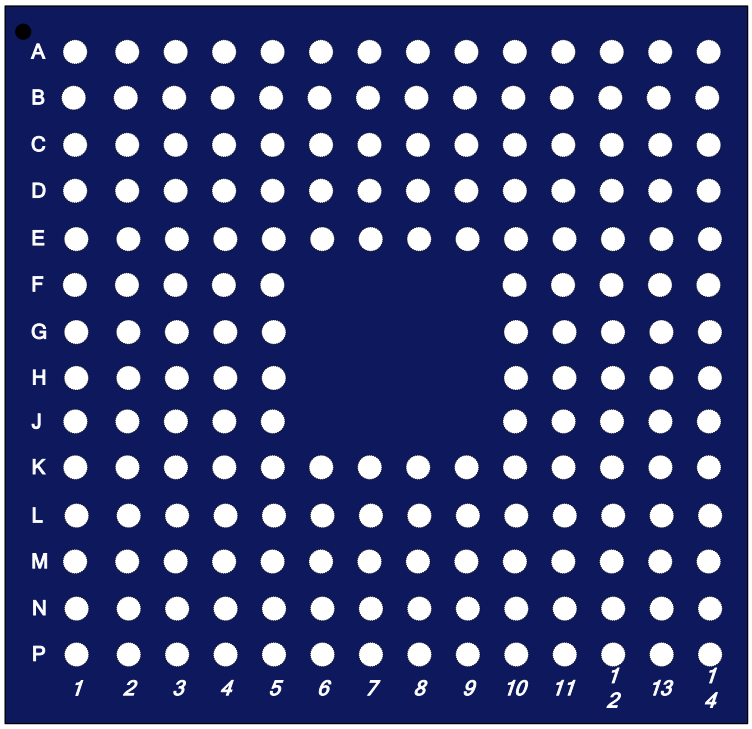
6 System Pins

6.1 System Diagram



6.2 Pin Description

6.2.1 Top View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PIOVDD	PIOVDD	TI2CD	TI2CC	SPIDI	PWR0	PWR1	SDDO15	SDDO8	GDRL	DRVIOVDD	DRVIOVDD	DRVIOVDD	DRVIOVDD
B	PIOVDD	SPIDO	SPICLK	SPICS1	PWR2	RES	GDOE	SDDO14	SDDO0	GDSP	SDOED	SDCEL5	DRVIOVDD	DRVIOVDD
C	PIOVDD	PWRCOM	PWR3	BDR0	BDR1	SDDO1	SDDO12	SDDO9	SDDO2	SDOE	SDDO3	SDCEL6	DRVIOVDD	DRVIOVDD
D	SPICS0	GPIO3	COREVDD	HIOVDD	RES	SDDO11	SDDO13	SDDO10	COREVDD	COREVDD	COREVDD	SDOEX	SDCEL3	SDCEL0
E	GPIO2	HIRQ	OSCVSS	HIOVDD	VSS	VSS	VSS	VSS	VSS	VSS	COREVDD	SDCEL4	SDDO7	SDSHR
F	GPIO0	OSCI	OSCVDD	PLLVSS	HIOVDD	AVT6203A				VSS	SDLE	SDCEL2	TRST	SDCLK
G	GPIO4	HDB14	OSCO	PLLVDD	HIOVDD					VSS	RES	SDDO4	GDCLK	SDDO6
H	HWEL	RES	HRDY	COREVDD	VSS					VSS	COREVDD	RES	RES	SDDO5
J	CNF2	HRDL	GPIO1	HDB0	VSS					VSS	COREVDD	VSS	VSS	SDCEL1
K	HD/C	HCSL	HDB15	HDB1	VSS	VSS	VSS	VSS	VSS	VSS	COREVDD	COREVDD	SDRVDD	SDRVDD
L	CLKI	HDB10	GPIO5	HDB4	VSS	SDRVDD	SDRVDD	SDRVDD	SDRVDD	VSS	VSS	VSS	SDRVDD	SDRVDD
M	HDB13	HDB12	RESETL	HDB6	VSS	SDRVDD	SDRVDD	SDRVDD	SDRVDD	VSS	VSS	VSS	VSS	VSS
N	HDB11	HDB3	HDB7	HDB5	VSS	SDRVDD	SDRVDD	SDRVDD	SDRVDD	VSS	VSS	VSS	VSS	VSS
P	HDB8	HDB2	HDB9	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS

6.2.2 System Clock Interface

Pin Name	I/O	BALL NAME	Description
CLKI*	I	L1	Clock input pin
OSCI*	I	F2	Crystal input pin
OSCO	O	G3	Crystal output pin
CNF2	I	J1	Input clock select pin = 1，OSC is clock input = 0，CLKI is clock input

***If OSC is clock input, CLKI must be pull high or pull-low.**

***If CLKI is clock input, OSCI must be pull-high or pull-low.**

6.2.3 Host Interface

Pin Name	I/O	BALL NAME	Description
HDB[15:0]	IO	K3, G2, M1, M2, N1, L2, P3, P1, N3, M4, N4, L4, N2, P2, K4, J4	Data bus for data/command transfer
HWEL	I	H1	Write enable pin (Low active)
HRDL	I	J2	Read enable pin (Low active)
HCSL	I	K2	Chip select pin (Low active)
HD/C	I	K1	Data/Command select pin
HRDY	O	H3	Chip busy pin
RESETL	I	M3	System reset pin (Low active)
HIRQ	O	E2	Interrupt pin

6.2.4 SPI Flash Interface

Pin Name	I/O	BALL NAME	Description
SPICS1	O	B4	SPI FLASH Chip select 1
SPICS0	O	D1	SPI FLASH Chip select 0
SPICLK	O	B3	SPI FLASH Clock input
SPIDO	O	B2	SPI FLASH data output
SPIDI	I	A5	SPI FLASH data input

6.2.5 I2C Interface

Pin Name	I/O	BALL NAME	Description

TI2CC	IO	A4	I2C clock pin
TI2CD	IO	A3	I2C data pin

6.2.6 Source Driver Interface

Pin Name	I/O	BALL NAME	Description
SDCLK	O	F14	Source Driver Clock output
SDLE	O	F11	Source Driver Latch up
SDDO[15:0]	O	A8, B8, D7, C7, D6, D8, C8, A9, E13, G14, H14, G12, C11, C9, C6, B9	Source Driver data output.
SDOED	O	B11	Double data rate output
SDOEX	O	D12	Double data rate output
SDCEL[6:0]	O	C12, B12, E12,D13, F12, J14, D14	Source Driver chip select pins
SDSHR	O	E14	Source Driver shift pin
SDOE	O	C10	Source Driver output enable pin

6.2.7 Gate Driver Interface

Pin Name	I/O	BALL NAME	Description
GDCLK	O	G13	Gate Driver clock output
GDSP	O	B10	Gate Driver start pulse
GDOE	O	B7	Gate Driver output enable
GDRL	O	A10	Gate Driver shift control
BDR[1:0]	O	C5, C4	Display Border pin

6.2.8 Power Control Interface

Pin Name	I/O	BALL NAME	Description
PWR0	O	A6	Power 0 control
PWR1	O	A7	Power 1 control
PWR2	O	B5	Power 2 control
PWR3	O	C3	Power 3 control
PWRCOM	O	C2	Power COM control

6.2.9 Power Interface

Pin Name	I/O	BALL NAME	Description

HIOVDD	P	D4, E4, F5, G5	Host Interface power supply
PIOVDD	P	A1, A2, B1, C1	SPI,I2C Interface Power supply
COREVDD	P	D3, H4, D9, D10, D11, E11, H11, J11, K11, K12	CORE power supply
SDRVDD	P	L6, M6, N6, L7, M7, N7, L8, M8, N8, L9, M9, N9, K13, L13, K14, L14	SDRAM IO power supply
DRVIOVDD	P	A11, A12, A13, B13, C13, A14, B14, C14	Panel Interface power supply
PLLVDD	P	G4	PLL power supply
PLLVSS	G	F4	PLL ground
OSCVDD	P	F3	OSC power supply
OSCVSS	G	E3	OSC ground
VSS	G	P4, E5, H5, J5, K5, L5, M5, N5, P5, E6, K6, P6, E7, K7, P7, E8, K8, P8, E9, K9, P9, E10, F10, G10, H10, J10, K10, L10, M10, N10, P10, L11, M11, N11, P11, J12, L12, M12, N12, P12, J13, M13, N13, P13, M14, N14, P14	Digital ground

6.2.10 GPIO Interface

Pin Name	I/O	BALL NAME	Description
GPIO[5:0]	I/O	L3, G1, D2, E1, J3, F1	General IO

6.2.11 Others Pins

Pin Name	I/O	BALL NAME	Description
RES	I/O	H2, D5, B6, G11, H12, F13, H13	System reserve and must be floating.

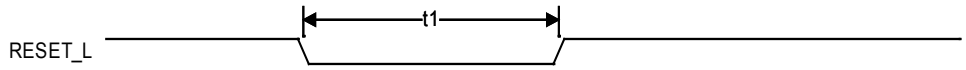
7 Power Supply

7.1 Recommend Power Condition

Symbol	Parameter	Condition	Min	Typ	Max	Units
Operating Temperature			-40	25	85	℃
COREVDD	Core Supply Voltage	Vss=0V	1.62	1.80	1.98	V
PIOVDD	SPI,I2C Supply Voltage	Vss=0V	2.70	3.30	3.60	V
HIOVDD	Host Supply Voltage	Vss=0V	1.62	1.80	1.98	V
		Vss=0V	2.70	3.30	3.60	V
SDRVDD	SDRAM IO Supply Voltage	Vss=0V	1.62	1.80	1.98	V
DRIOVDD	Panel Supply Voltage	Vss=0V	2.70	3.30	3.60	V
PLLVDD	PLL Supply Voltage	AVss=0V	1.62	1.80	1.98	V
OSCVDD	OSC Supply Voltage	Vss=0V	1.62	1.80	1.98	V

8 Interface Timing

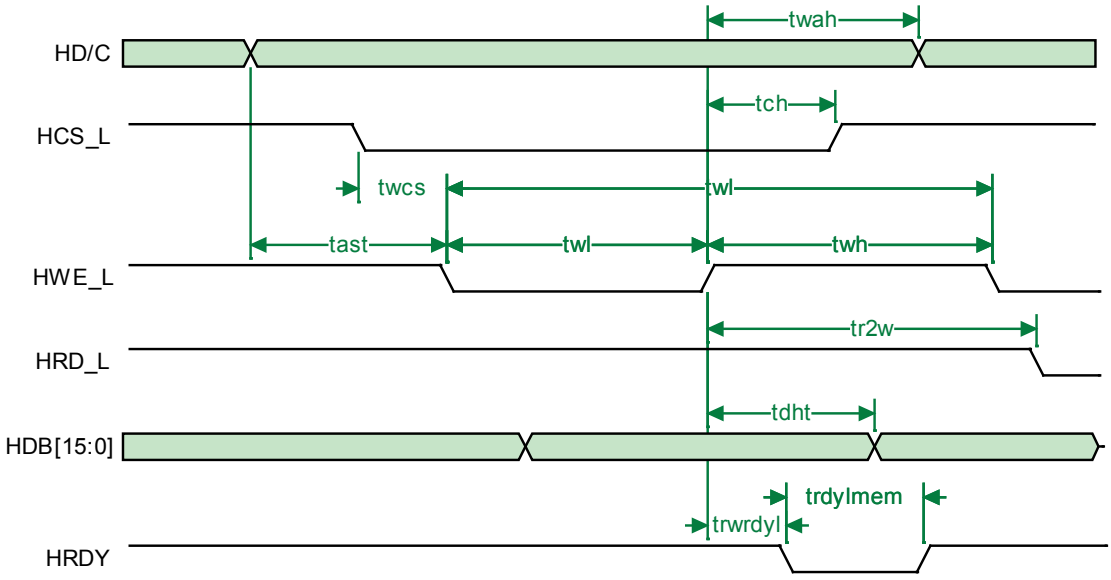
8.1 Reset Timing



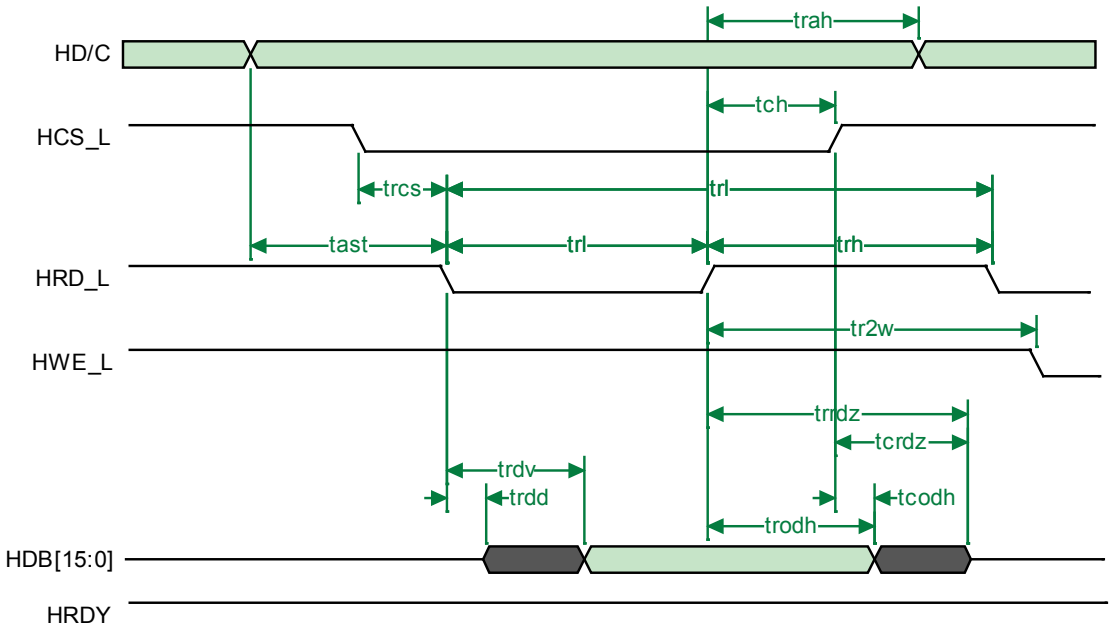
Symbol	Parameter	Min	Max	Units
t1	CLKI is system clock input	200	—	ns
	OSC is system clock input	4	—	ms

8.2 Host Interface Timing

8.2.1 16-bit Host Write Timing (Intel 80)



8.2.2 16-bit Host Read Timing (Intel 80)

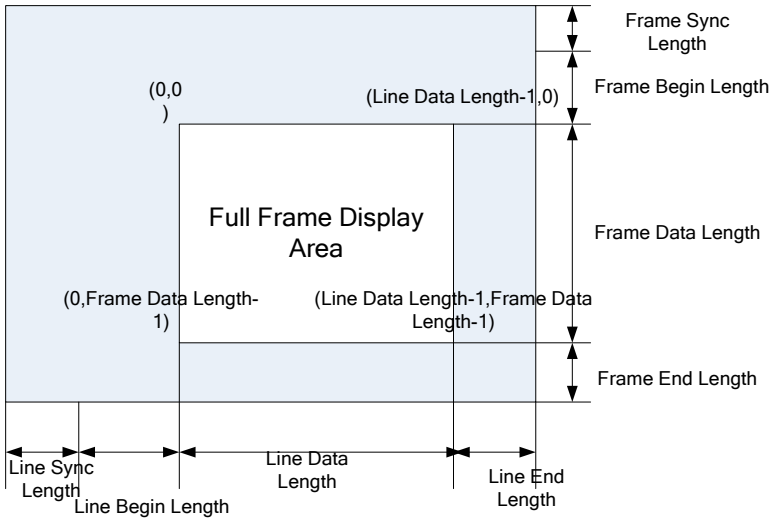


Signal	Symbol	Parameter	Min	Max	Unit	Description
HD/C	tast	Address setup time (read/write)	0	—	ns	
	twah	Address hold time (write)	5	—	ns	
	trah	Address hold time (read)	6	—	ns	
HCS_L	twcs	Chip Select setup time to HWR_L falling edge	1	—	ns	
	trcs	Chip Select setup time to HRD_L falling edge	1	—	ns	
	tch	Chip Select hold time (read/write)	5	—	ns	
HWE_L	twl	Pulse low duration	7	—	ns	
	twh	Pulse high duration	7	—	ns	
	twc	Write cycle for Registers	5	—	Ts	Ts = System Clock Cycle
		Write cycle for Memory	4	—	Ts	
	tw2r	HWR_L rising edge to HRD_L falling edge	2	—	Ts	
HRD_L	tr2w	HRD_L rising edge to HWR_L falling edge	0	—	ns	
	trc	Read cycle for Registers	5	—	Ts	Ts = System Clock Cycle
		Read cycle for Memory	4	—	Ts	

	trl	Pulse low duration (for Registers)	4T + 24	—	ns	
		Pulse low duration (for Memory)	3T + 23	—	ns	
	trh	Pulse high duration	4	—	ns	
HDB[15:0]	tdst	Write data setup time	7	—	ns	
	tdht	Write data hold time	6	—	ns	
	trodh	Read data hold time from HRD_L rising edge	2	9	ns	
	trrdz	HRD_L rising edge to HDB[15:0] Hi-Z	2	9	ns	
	trdv	HRD_L falling edge to HDB[15:0] valid for Registers	—	4T + 23	ns	CL=30pF
		HRD_L falling edge to HDB[15:0] valid for Memory (if trc not met)	—	3T + 22	ns	
	trdd	HRD_L falling edge to HDB[15:0] driven	4	—	ns	CL=30pF
HRDY	trwrdyl	HWE_L rising edge to HRDY falling edge	—	17	ns	CL=30pF
	trdylmem	HRDY low period for memory Write	—	3	Ts	CL=30pF

8.3 Panel Interface

8.3.1 Setting Diagram



8.3.2 Frame Rate Calculation

$$PixelClkFrequency = \frac{SystemClkFrequency}{PixelClkDivideSelected(REG18)}$$

$$SourceDriverClkFrequency = \frac{PixelClkFrequency}{PixelPerClockOutputSelect(REG030C[11])}$$

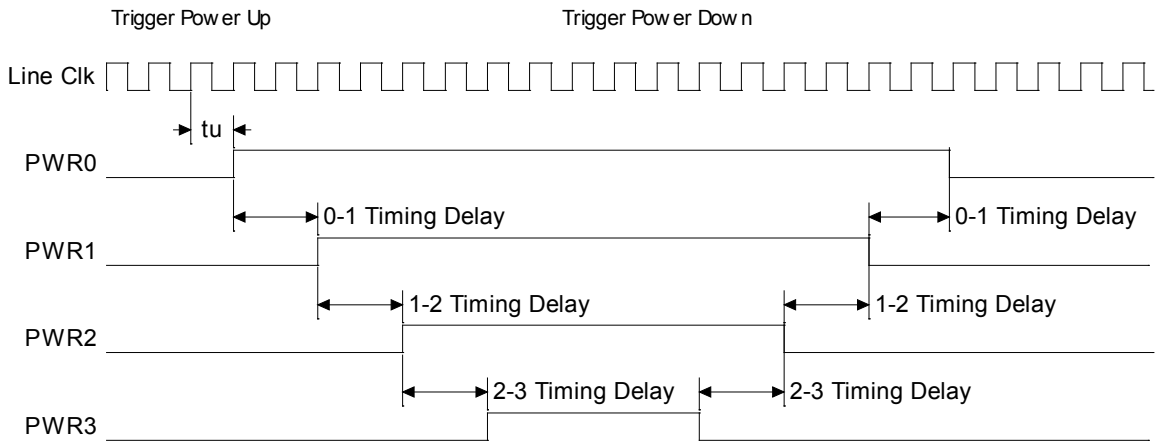
$$HorizontalTotalPixel = LineSyncLength + LineBeginLength + LineDataLength + LineEndLength$$

$$GateDriveGDCLKFrequency = \frac{SourceDriverClkFrequency}{HorizontalTotalPixel} MHz$$

$$VerticalTotalLines = FrameSyncLength + FrameBeginLength + FrameDataLength + FrameEndLength$$

$$FrameRate = \frac{GDCLKFrequency}{VerticalTotalLines}$$

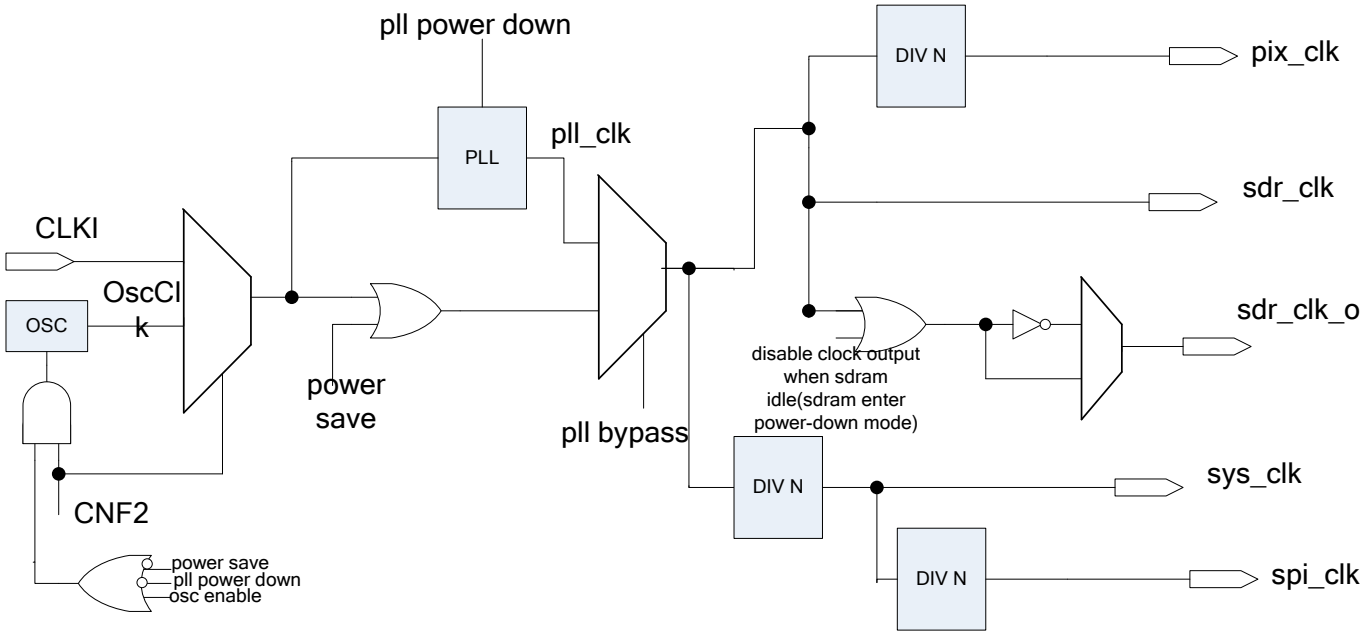
8.4 Power Pin Interface



Symbol	Parameter	Min	Max	Units
tu	Trigger Power up to Power Pin 0 transition	0	1	Source CLK
0-1Timing Delay	Power pin 0 to Power pin 1 Timing Delay	1	REG[0234h]	512 * Source CLK
1-2Timing Delay	Power pin 1 to Power pin 2 Timing Delay	1	REG[0236h]	512 * Source CLK
2-3Timing Delay	Power pin 2 to Power pin 3 Timing Delay	1	REG[0238h]	512 * Source CLK

9 Clock

9.1 Clock description

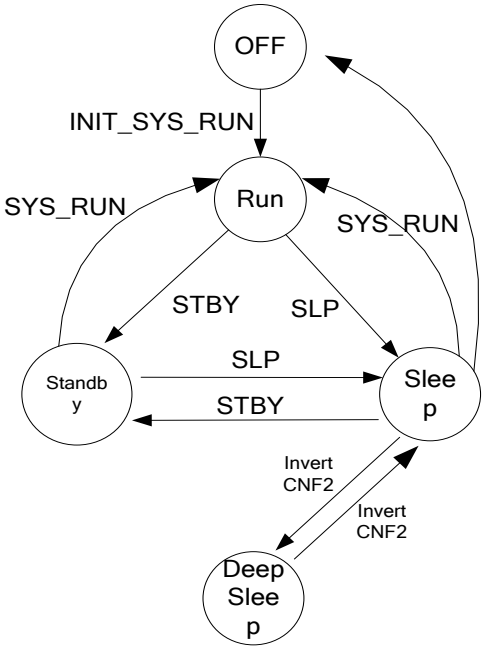


9.2 Power Manager

9.2.1 Power Mode Description

Power Mode	Controller State	PLL State	SDRAM State	SDRAM Data Retained	Power Consumption
OFF	Unknown	Unknown	Unknown	No	NA
Run	Active All clocks active	Active	Normal Operation	Yes	High
Standby	Power Save Mode All module clocks gated off PLL is running	Active	Self Refresh	Yes	Low
Sleep	Power Save Mode Power Pin cycle off PLL off	Powered-Down	Self Refresh	Yes	Lower
Deep Sleep	Power Save Mode Power Pin cycle off PLL off Clock input Disable	Powered-Down	Self Refresh	Yes	Lowest

9.2.2 Power Mode Convert Diagram



9.2.3 Power Mode Convert:

Current State	Next State Requirements				
	Off	Run	Standby	Sleep	Deep Sleep
Off	NA	1. Power on Reset 2. Run INIT_SYS_RUN	Not Possible.	Not Possible.	Not Possible.
Run	1. Host Save Memory Contents 2. Run SLP 3. Power off	NA	1. Run STBY	1. Run SLP	1. Run SLP 2. Invert CNF2
Standby	1. Run CMD SLP 2. Power off	1. Run RUN_SYS	NA	1. Run CMD SLP	1. Run SLP 2. Invert CNF2
Sleep	1. Power off	1. Run RUN_SYS	1. Run CMD STBY	NA	1. Invert CNF2
Deep sleep	1. Power off	1. Invert CNF2 2. Run RUN_SYS	1. Invert CNF2 2. Run STBY	1. Invert CNF2	NA

Current State	Estimated Transition Time				
	Off	Run	Standby	Sleep	Deep sleep
Off	NA	20ms	NA	NA	NA
Run	NA	NA	1us	1us	1us
Standby	NA	1us	NA	1us	1us
Sleep	NA	1ms	1us	NA	1us
Deep sleep	NA	1ms	1us	1us	NA

10 Command List

Code	Command	Parameters				
		1	2	3	4	5
System commands						
0x00	INIT_CMD_SET	SPI_CFG	SFM [15:0]	SFM [23:16]		
0x01	INIT_PLL_STBY	PLL_CFG0	PLL_CFG1	PLL_CFG2		
0x02	RUN_SYS					
0x04	STBY					
0x05	SLP					
0x06	INIT_SYS_RUN					
0x07	INIT_SYS_STBY					
0x08	INIT_SDRAM	SDRAMCFG0	SDRAMCFG1	SDRAMCFG2	SDRAMCFG3	
0x09	INIT_DSPE_CFG	HSIZE	VSIZE	SDRVCFG	GDRVCFG	LUT index Format CFG
0x0A	INIT_DSPE_TMG	Frame Sync CFG	Frame Begin/End CFG	Line Sync CFG	Line Begin/End CFG	Pixel Clock CFG
0x0B	INIT_ROTMODE	ROTMODE				
Register and Memory Access Commands						
0x10	RD_REG	REGADDR[15:0]	RDATA[15:0]			
0x11	WR_REG	REGADDR[15:0]	WDATA[15:0]			
0x12	RD_SFM					
0x13	WR_SFM	WDATA[15:0]				
0x14	END_SFM					
Burst Access Commands						
0x1C	BST_RD_SDR	MA[15:0]	MA[25:16]	BC[15:0]	BC[25:16]	
0x1D	BST_WR_SDR	MA[15:0]	MA[25:16]	BC[15:0]	BC[25:16]	
0x1E	BST_END_SDR					
IMAGE LOADING COMMANDS						
0x20	LD_IMG	ARG[15:0]				
0x22	LD_IMG_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]
0x23	LD_IMG_END					
0x24	LD_IMG_WAIT					
0x25	LD_IMG_SETADR	MA[15:0]	MA[25:16]			
0x26	LD_IMG_DSPEADR					
Polling commands						
0x28	WAIT_DSPE_TRG					
0x29	WAIT_DSPE_FREND					
0x2A	WAIT_DSPE_LUTFREE					
0x2B	WAIT_DSPE_MLUTFREE	LUT MASK				

Waveform Update Commands						
0x30	RD_WFM_INFO	MA[15:0]	MA[23:16]			
0x32	UPD_INIT					
0x33	UPD_FULL	ARG[15:0]				
0x34	UPD_FULL_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]
0x35	UPD_PART	ARG[15:0]				
0x36	UPD_PART_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]
0x37	UPD_GDRV_CLR					
0x38	UPD_SET_IMGADR	ADR[15:0]	ADR[31:16]			
Image Processing Command						
0x3A	DITHER_SET_ADR	ADR[15:0]	ADR[31:16]			
0x3B	DITHER_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]

10.1 Commands Description

10.1.1 INIT_CMD_SET

Initial the instruction table and register.

	Code	Command	Parameter 1	Parameter 2	Parameter 3
	0x00	INIT_CMD_SET	SPI_CFG	SFM [15:0]	SFM [23:16]
Register			[0204h]		
Bit			[7:0]	[15:0]	[7:0]

10.1.2 INIT_PLL_STBY

Initial PLL and set the chip to standby mode.

	Code	Command	Parameter 1	Parameter 2	Parameter 3
	0X01	INIT_PLL_STBY	PLL_CFG0	PLL_CFG1	PLL_CFG2
Register			[0010h]	[0012h]	[0014h]
Bit			[5:0]	[15:12]	[7:3]

10.1.3 RUN_SYS

Wake up the chip from standby or sleep mode.

	Code	Command
	0x02	RUN_SYS
Register		
Bit		

10.1.4 STBY

Set the chip into standby mode from run mode.

	Code	Command
	0x04	STBY
Register		
Bit		

10.1.5 SLP

Set the chip into sleep mode from run mode.

	Code	Command
	0x05	SLP
Register		
Bit		

10.1.6 INIT_SYS_RUN

Initial all registers to known status and set system to run mode.

	Code	Command
	0x06	INIT_SYS_RUN
Register		
Bit		

10.1.7 INIT_SYS_STBY

Initial all registers to known status and set system to standby mode.

	Code	Command
	0x07	INIT_SYS_STBY
Register		
Bit		

10.1.8 INIT_SDRAM

Initial SDRAM to known status.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4
	0x08	INIT_SDRAM	SDRAMCFG0	SDRAMCFG1	SDRAMCFG2	SDRAMCFG3
Register			[0100h]	[0106h]	[0108h]	[010Ah]
Bit			[15:4] [2:0]	[15:0]	[5:4]	[14:8] [2:0]

10.1.9 INIT_DSPE_CFG

Initial the display engine configuration.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5
	0x09	INIT_DSPE_CFG	HSIZE	VSIZE	SDRVCFG	GDRVCFG	LUT index Format CFG
Register			[0306h]	[0300h]	[030Ch]	[030Eh]	[0330h]
Bit			[12:0]	[12:0]	[15:0]	[15:3] [1:0]	[15] [7:6] [2:0]

10.1.10 INIT_DSPE_TMG

Initial the display engine timing.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5
	0x0A	INIT_DSPE_TMG	Frame Sync CFG	Frame Begin /End CFG	Line Sync CFG	Line Begin /End CFG	Pixel Clock CFG
Register			[0302h]	[0304h]	[0308h]	[030Ah]	[0018h]
Bit			[7:0]	[15:0]	[7:0]	[15:0]	[4:0]

10.1.11 INIT_ROTMODE

Initial the display rotation mode.

	Code	Command	Parameter 1
	0x0B	INIT_ROTMODE	ROTMODE
Register			[032Ch]
Bit			[9:8]

10.1.12 RD_REG

Read the register.

	Code	Command	Parameter 1	Parameter 2
	0x10	RD_REG	REGADDR[15:0]	RDATA[15:0]
Register				
Bit			[15:0]	[15:0]

10.1.13 WR_REG

Write the register.

	Code	Command	Parameter 1	Parameter 2

	0x11	WR_REG	REGADDR[15:0]	WDATA[15:0]
Register				
Bit			[15:0]	[15:0]

10.1.14 RD_SFW

Set the chip to read the SPI flash.

	Code	Command
	0x12	RD_SFM
Register		
Bit		

10.1.15 WR_SFW

Set the chip to write the SPI flash.

	Code	Command	Parameter 1
	0x13	WR_SFM	WDATA[15:0]
Register			
Bit			[15:0]

10.1.16 END_SFW

Stop operation for SPI flash.

	Code	Command
	0x14	END_SFM
Register		
Bit		

10.1.17 BST_RD_SDR

Set the memory control to burst read.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4
	0x1C	BST_RD_SDR	MA[15:0]	MA[25:16]	BC[15:0]	BC[25:16]
Register			[0144h]	[0146h]	[0148h]	[014Ah]
Bit			[15:0]	[7:0]	[15:0]	[9:0]

10.1.18 BST_WR_SDR

Set the memory control to burst write.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4

	0x1D	BST_WR_SDR	MA[15:0]	MA[25:16]	BC[15:0]	BC[25:16]
Register			[0144h]	[0146h]	[0148h]	[014Ah]
Bit			[15:0]	[7:0]	[15:0]	[9:0]

10.1.19 BST_END_SDR

Stop operation for SDRAM.

	Code	Command
	0x1E	BST_END_SDR
Register		
Bit		

10.1.20 LD_IMG

Set full image information for display.

	Code	Command	Parameter 1
	0x20	LD_IMG	ARG[15:0]
Register			[0140h]
Bit			[5:4]

10.1.21 LD_IMG_AREA

Set part image information for display.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5
	0x22	LD_IMG_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]
Register			[0140h]	[014Ch]	[014Eh]	[0150h]	[0152h]
Bit			[5:4]	[11:0]	[11:0]	[12:0]	[12:0]

10.1.22 LD_IMG_END

Notification the load image process will be stopped.

	Code	Command
	0x23	LD_IMG_END
Register		
Bit		

10.1.23 LD_IMG_WAIT

Notification the load image process will be stopped and wait the processor is done.

	Code	Command
	0x24	LD_IMG_WAIT
Register		
Bit		

10.1.24 LD_IMG_SETADR

Set the image address of SDRAM.

	Code	Command	Parameter 1	Parameter 2
	0x25	LD_IMG_SETADR	MA[15:0]	MA[25:16]
Register			[0144h]	[0146h]
Bit			[15:0]	[9:0]

10.1.25 LD_IMG_DSPEADR

Synchronous the load image address and display image address register.

	Code	Command
	0x26	LD_IMG_DSPEADR
Register		
Bit		

10.1.26 WAIT_DSPE_TRG

Wait display engine data process done.

	Code	Command
	0x28	WAIT_DSPE_TRG
Register		
Bit		

10.1.27 WAIT_DSPE_FREND

Wait display done.

	Code	Command
	0x29	WAIT_DSPE_FREND
Register		
Bit		

10.1.28 WAIT_DSPE_LUTFREE

Wait a LUT is free.

	Code	Command
	0x2A	WAIT_DSPE_LUTFREE
Register		
Bit		

10.1.29 WAIT_DSPE_MLUTFREE

Wait the customer LUT is free.

	Code	Command	Parameter 1
	0x2B	WAIT_DSPE_MLUTFREE	LUT MASK
Register			[032Eh]
Bit			[15:0]

10.1.30 RD_WFM_INFO

Set waveform start address at SPI flash.

	Code	Command	Parameter 1	Parameter 2
	0x30	RD_WFM_INFO	MA[15:0]	MA[23:16]
Register			[0350h]	[0352h]
Bit			[15:0]	[7:0]

10.1.31 UPD_INIT

Synchronous the SDRAM to customer data.

	Code	Command
	0X32	UPD_INIT
Register		
Bit		

10.1.32 UPD_FULL

Display full image by refresh mode.

	Code	Command	Parameter 1
	0x33	UPD_FULL	ARG[15:0]
Register			[0334h]
Bit			[14] [11:4]

10.1.33 UPD_FULL_AREA

Display part image by custom setting.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5
	0x34	UPD_FULL_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]
Register			[0334h]	[0340h]	[0342h]	[0344h]	[0346h]
Bit			[14] [11:4]	[11:0]	[11:0]	[12:0]	[12:0]

10.1.34 UPD_PART

Display full image by mode.

	Code	Command	Parameter 1
	0x35	UPD_PART	ARG[15:0]
Register			[0334h]
Bit			[14] [11:4]

10.1.35 UPD_PART_AREA

Display part image by custom setting.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5
	0x36	UPD_PART_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]
Register			[0334h]	[0340h]	[0342h]	[0344h]	[0346h]
Bit			[14] [11:4]	[11:0]	[11:0]	[12:0]	[12:0]

10.1.36 UPD_GDRV_CLR

Clear gate driver status when the power on.

	Code	Command
	0x37	UPD_GDRV_CLR
Register		
Bit		

10.1.37 UPD_SET_IMGADR

Set display image address of SDRAM.

	Code	Command	Parameter 1	Parameter 2
	0x38	UPD_SET_IMGADR	ADR[15:0]	ADR[31:16]

Register			[0310h]	[0312h]
Bit			[15:0]	[15:0]

10.1.38 DITHER_SET_ADR

Set Dithering image address of SDRAM.

	Code	Command	Parameter 1	Parameter 2
	0x3A	DITHER_SET_ADR	ADR[15:0]	ADR[31:16]
Register			[0420h]	[0422h]
Bit			[15:0]	[15:0]

10.1.39 DITHER_AREA

Set Dithering mode and image area.

	Code	Command	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5
	0x3B	DITHER_AREA	ARG[15:0]	XSTART[11:0]	YSTART[11:0]	WIDTH[12:0]	HEIGHT[12:0]
Register			[0400h]	[0410h]	[0412h]	[0414h]	[0416h]
Bit			[2:1] [0]	[11:0]	[11:0]	[12:0]	[12:0]

11 Register

11.1 Register List

Address	Description
0000h to 000Ah	System Configuration Register
0010h to 001Ah	Clock Configuration Register
0020h	Memory Load Configuration Register
0030h	Driver Strength Configuration Register
0100h to 010Ch	SDRAM Configuration Register
0140h to 01A0h	HOST Memory Configuration Register
0200h to 0208h	SPI Flash Configuration Register
0210h to 021Ah	I2C Configuration Register
0230h to 0238h	Power Pin Configuration Register
0240h to 0244h	Interrupt Configuration Register
0250h to 0258h	GPIO Configuration Register
0290h to 0294h	Command RAM Configuration Register
0300h to 030Ah	Display Timing Configuration Register
030Ch to 030Eh	Source Driver Configuration Register
0310h to 0316h	Display Buffer Configuration Register
0320h to 032Eh	General Configuration Register
0330h to 0334h	Update Buffer Configuration Register
0336h to 0338h	LUT Status Register
033Ah to 033Eh	Interrupt Register
0340h to 034Eh	Display Engine Configuration Register
0350h to 0352h	SPI Flash Start Address Configuration Register
0370h to 0372h	Advanced Display Configuration Register
0380h to 0392h	AUO Configuration Registers
0400h to 0422h	Dithering Configuration Registers
0800h	Instruction Parameter Configuration Register

11.2 Register Description

11.2.1 System Configuration Register

11.2.1.1 [0000h]Revision Code Register

15	14	13	12	11	10	9	8
Revision code							
7	6	5	4	3	2	1	0
Revision code							

Bit	Name	Description	R/W	Reset Value
15:0	Revision code	Revision Code	R	0x0000

11.2.1.2 [0002h]Product Code Register

15	14	13	12	11	10	9	8
Product code							
7	6	5	4	3	2	1	0
Product code							

Bit	Name	Description	R/W	Reset Value
15:0	Product code	Product Code	R	0000_0000_ 0100_0111

11.2.1.3 [0006h]Power Save Mode Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Power save mode enable

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System Reserved	R	0000_0000_ 0000_000
0	Power save mode enable	[0] = 0, Disable power save mode [0] = 1, Enable power save mode	R/W	0

11.2.1.4 [0008h] Software Reset Register

15	14	13	12	11	10	9	8
Software reset							
7	6	5	4	3	2	1	0
Software reset							

Bit	Name	Description	R/W	Reset Value
15:0	Software Reset	Reset all registers to default value	W	0000_0000_ 0000_0000

11.2.1.5 [000Ah]System Statue Register

15	14	13	12	11	10	9	8
Reserved	Power management busy status	Reserved		Power save status		SDRAM self refresh mode register	Power sequence status
7	6	5	4	3	2	1	0
I2C busy status	SPI busy status	Host interface busy status	SDRAM controller busy status	Host memory access busy status	Display engine busy status	SDRAM initialized	PLL Lock Status

Bit	Name	Description	R/W	Reset Value
15	Reserved	System Reserved	R	0
14	Power management busy status	[14] = 0, Power pin idle。 [14] = 1, Power pin busy。	R	0
13:12	Reserved	System reserved	R	0
11:10	Power save status	[11:10] Power Save Status 00b Un-initalized System 01b Run Mode 10b Standby Mode 11b Sleep Mode	R	00
9	SDRAM self refresh mode register	[9] = 0, SDRAM isn't in self refresh mode [9] = 1, SDRAM is in self refresh mode	R	0
8	Power sequence status	[8] = 0, Power off status. [8] = 1, Power on status	R	0
7	I2C busy status	[7] = 0, I2C interface idle. [7] = 1, I2C interface busy.	R	0
6	SPI busy status	[6] = 0, SPI interface idle. [6] = 1, SPI interface busy.	R	0

Bit	Name	Description	R/W	Reset Value
5	Host interface busy status	[5] = 0, Host interface idle. [5] = 1, Host interface busy.	R	0
4	SDRAM controller busy status	[4] = 0, SDRAM controller idle. [4] = 1, SDRAM controller busy.	R	0
3	Host memory access busy status	[3] = 0, Host memory idle. [3] = 1, Host memory busy.	R	0
2	Display engine busy status	[2] = 0, Display engine idle. [2] = 1, Display engine busy.	R	0
1	SDRAM initialized	[1] = 0, SDRAM is not initialed. [1] = 1, SDRAM is initialed.	R	0
0	PLL Lock Status	[0] = 0, PLL don't lock. [0] = 1, PLL lock.	R	0

11.2.2 Clock configuration Register

11.2.2.1 [0010h] PLL Configuration Registers 0

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		Lock time [5:0]					

Bit	Name	Description	R/W	Reset Value
15:6	Reserved	System Reserved	R	0000_0000_00
5:0	Lock time	PLL lock time is 500us P = input clock frequency (ms) [5:0] = roundup [500/(2x1024xP)]	R/W	00000

11.2.2.2 [0012h] PLL Configuration 1

15	14	13	12	11	10	9	8
VCO Kv setting				Reserved			
7	6	5	4	3	2	1	0
Reserved							

Bit	Name	Description	R/W	Reset Value
15:12	VCO Kv Setting	[15:12] = 0100, 100MHz =< output frequency < 120MHz. [15:12] = 0101, 120MHz =< output frequency < 133MHz.	R/W	0
11:0	Reserved	System reserved	R	0

11.2.2.3 [0014h] PLL Configuration 2

15	14	13	12	11	10	9	8
M setting							
7	6	5	4	3	2	1	0
N setting							K

Bit	Name	Description	R/W	Reset Value
15:8	M Setting	Output clock frequency = input clock frequency * M/(N*(1+K))	R/W	00001000
7:1	N Setting		R/W	0000010
0	K		R/W	0

11.2.2.4 [0016h] Clock Configuration Register

15	14	13	12	11	10	9	8
Reserved						System clock divider select	
7	6	5	4	3	2	1	0
Reserved						PLL power down enable	PLL bypass mode enable

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9:8	System clock divider Select	[9:8] = 00b: 2:1 [9:8] = 01b: 3:1 [9:8] = 10b: 1:1 [9:8] = 11b: 1:1	R/W	00
7:2	Reserved	System reserved	R	0000_00
1	PLL power down enable	[1] = 0, PLL is in active mode. [1] = 1, PLL is in power down mode.	R/W	1
0	PLL bypass mode enable	[0] = 0, PLL bypass disable. [0] = 1, PLL bypass enable.	R/W	1

11.2.2.5 [0018h] Pixel Clock Configuration Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				Pixel clock divide select			

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>15:4</td><td>Reserved</td><td>System reserved</td><td>R</td><td>0000_0000_
0000</td></tr>
<tr><td>3:0</td><td>Pixel clock divide select</td><td><table><tr><th>[3:0]</th><th>Pixel Clock Divide Ratio</th></tr><tr><td>0000b</td><td>4:1</td></tr><tr><td>0001b</td><td>2:1</td></tr><tr><td>0010b</td><td>3:1</td></tr><tr><td>0011b</td><td>4:1</td></tr><tr><td>0100b</td><td>5:1</td></tr><tr><td>0101b</td><td>6:1</td></tr><tr><td>0110b</td><td>7:1</td></tr><tr><td>0111b</td><td>8:1</td></tr><tr><td>1000b</td><td>9:1</td></tr><tr><td>1001b</td><td>10:1</td></tr><tr><td>1010b</td><td>11:1</td></tr><tr><td>1011b</td><td>12:1</td></tr><tr><td>1100b</td><td>13:1</td></tr><tr><td>1101b</td><td>14:1</td></tr><tr><td>1110b</td><td>16:1</td></tr><tr><td>1111b</td><td>64:1</td></tr></table></td><td>R/W</td><td>0000</td></tr>
</table>

11.2.2.6 [001Ah] I2C Thermal Sensor Clock Configuration

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				Thermal sensor clock divide select			

Bit	Name	Description	R/W	Reset Value
15:4	Reserved	System reserved	R	0000_0000_ 0000
3:0	Thermal sensor clock divide select	System clock : I2C clock = ([3:0] + 1) x 32) : 1	R/W	0000

11.2.3 Memory Load Configuration Register

11.2.3.1 [0020h] Memory Load Configuration Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						Big median	Reserved

	memory load enable	

Bit	Name	Description	R/W	Reset Value
15:2	Reserved	System reserved	R	0000_0000_0000_00
1	Big endian memory load enable	Big Endian Memory Load Enable [1] = 0, Little Endian enable. [1] = 1, Big Endian enable.	R/W	0
0	Reserved	System reserved	R/W	0

11.2.4 Driver Strength Configuration Register

11.2.4.1 [0030h] Interface Driver Strength Configuration Register

15	14	13	12	11	10	9	8
Reserved				Host data interface driver strength set			Source/Gate interface driver strength set
7	6	5	4	3	2	1	0
Source/Gate interface driver strength set		SDRAM address interface driver strength set		SDRAM data interface driver strength set			

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:9	Host data interface driver strength set	Host data driver strength [11:9] – Driver strength 000b – 4mA 001b – 8mA 011b – 12mA 111b – 16mA	R/W	001
8:6	Source/Gate interface driver strength set	Source/Gate driver strength [8:6] – Driver strength 000b – 4mA 001b – 8mA 011b – 12mA 111b – 16mA		001
5:3	SDRAM address interface driver strength set	SDRAM address driver strength [5:3] – Driver strength 000b – 4mA 001b – 8mA		011

Bit	Name	Description	R/W	Reset Value
		011b 12mA 111b 16mA		
2:0	SDRAM data interface driver strength set	SDRAM data driver strength [2:0] Driver strength 000b 4mA 001b 8mA 011b 12mA 111b 16mA		011

11.2.5 SDRAM Configuration Register

11.2.5.1 [0100h] SDRAM Configuration Register

15	14	13	12	11	10	9	8
SDRAM power down disable	SDRAM refresh cycle time			SDRAM refresh rate		SDRAM row active time	
7	6	5	4	3	2	1	0
16 bit SDRAM enable	SDRAM trip latency select	SDRAM tRCD latency select	SDRAM tCL latency select	Reserved	SDRAM column address count		SDRAM burst type select

Bit	Name	Description	R/W	Reset Value
15	SDRAM power down disable	[15] = 0, SDRAM power down enable. [15] = 1, SDRAM power down disable.	R/W	0
14:12	SDRAM refresh cycle time	SDRAM tRFC Refresh cycle time = [14:12] + 4	R/W	101
11:10	SDRAM refresh rate	SDRAM refresh rate（8192 rows）. REG0100h [11:10] Refresh Ratio 00 64ms 01 128ms 10 256ms 11 512ms	R/W	00
9:8	SDRAM row active time	tRAS REG0100h [9:8] Row Active Time 00 5clocks 01 N/A 10 6 clocks 11 7 clocks	R/W	00
7	16 bit SDRAM	[7] = 0, SDRAM databus is 32-Bits.	R/W	0

Bit	Name	Description	R/W	Reset Value
	enable	[7] = 1, SDRAM databus is 16-Bits.		
6	SDRAM tRP latency select	[6] = 0, tRP is 2 clocks。 [6] = 1, tRP is 3 clocks。	R/W	1
5	SDRAM tRCD latency select	[5] = 0, tRCD is 2 clocks。 [5] = 1, tRCD is 3 clocks。	R/W	1
4	SDRAM tCL latency select	[4] = 0, tCL is 2 clocks。 [4] = 1, tCL is 3 clocks。	R/W	1
3	Reserved	System reserved	R	0
2:1	SDRAM column address count	REG0100h [2:1] / Column Address Count 00 / 256 01 / 512 10 / 1024 11 / 2048	R/W	00
0	SDRAM burst type select	[0] = 0, full page burst mode（For normal SDRAM）. [0] = 1, 8-burst mode（For mobile SDRAM）	R/W	0

11.2.5.2 [0102h] SDRAM Initial Register

15	14	13	12	11	10	9	8
Reserved							SDRAM initial complete
7	6	5	4	3	2	1	0
Reserved							SDRAM initial trigger

Bit	Name	Description	R/W	Reset Value
15:9	Reserved	System reserved	R	0000_000
8	SDRAM initial complete	[8] = 0, SDRAM has not been initialed. [8] = 1, SDRAM has been initialed.	R/W	0
7:1	Reserved	System reserved	R	0000_000
0	SDRAM initial trigger	[0] = 1, Set the bit to1 for trigger SDRAM initial.	R/W	0

11.2.5.3 [0104h] SDRAM State Trigger Register

15	14	13	12	11	10	9	8
Reserved							SDRAM self refresh mode state
7	6	5	4	3	2	1	0
Reserved						SDRAM exit self refresh	SDRAM enter

	trigger	self refresh trigger

Bit	Name	Description	R/W	Reset Value
15:9	Reserved	System reserved	R	0000_000
8	SDRAM self refresh mode State	[8] = 0, SDRAM is not in self refresh mode. [8] = 1, SDRAM is in self refresh mode.	R/W	0
7:2	Reserved	System reserved	R	0000_00
1	SDRAM exit self refresh trigger	[1] = 1, Set the bit to 1for disable SDRAM self refresh.	R/W	0
0	SDRAM enter self refresh trigger	[0] = 1, Set the bit to 1 for enable SDRAM self refresh	R/W	0

11.2.5.4 [0106h] SDRAM Refresh Clock Configuration Register

15	14	13	12	11	10	9	8
SDRAM refresh clock divide select							
7	6	5	4	3	2	1	0
SDRAM refresh clock divide select							

Bit	Name	Description	R/W	Reset Value
15:0	SDRAM refresh clock divide select	SDRAM refresh frequency = F(INPUTCLK)/([15:0] +1)	R/W	0000_0001_0111_0111

11.2.5.5 [0108h] SDRAM Read Data Delay Select Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		SDRAM read data sampling edge select	SDRAM read data sampling clock invert enable	Reserved			

Bit	Name	Description	R/W	Reset Value
15:6	Reserved	System reserved	R	0000_0000_00
5	SDRAM read data sampling edge select	[5] = 0, Posedge clock for data sampling [5] = 1, Negedge clock for data sampling.	R/W	0
4	SDRAM read data sampling clock invert	[4] = 0, Disable SDRAM read data sampling clock invert. [4] = 1, Enable SDRAM read data sampling clock invert.	R/W	0

Bit	Name	Description	R/W	Reset Value
	enable			
3:1	Reserved	System reserved	R	000

11.2.5.6 [010Ah] SDRAM Extended Mode Configuration Register

15	14	13	12	11	10	9	8
Reserved	SDRAM driver strength		Temperature compensated Self refresh		Partial array self refresh		
7	6	5	4	3	2	1	0
Reserved					SDRAM size		Extended mode register program on initialization enable

Bit	Name	Description	R/W	Reset Value
15	Reserved	System reserved	R	0
14:13	SDRAM driver strength	[14:13] = 00, full strength [14:13] = 01, 1/2 full strength [14:13] = 10, 1/4 full strength [14:13] = 11, 1/8 full strength	R/W	00
12:11	Temperature compensated self refresh	TCSR Configuration	R/W	00
10:8	Partial array self refresh	PASR Configuration	R/W	00
7:3	Reserved	System reserved	R	0000_0
2:1	SDRAM size	<table><tr><th>REG010Ah [2:1]</th><th>SDRAM Size for 32-bit SDRAM</th><th>SDRAM Size for 16-bit SDRAM</th></tr><tr><td>00</td><td>8M bytes</td><td>4M bytes</td></tr><tr><td>01</td><td>16M bytes</td><td>8M bytes</td></tr><tr><td>10</td><td>32M bytes</td><td>16M bytes</td></tr><tr><td>11</td><td>64M bytes</td><td>32M bytes</td></tr></table>	R/W	00
0	Extended mode register program on initialization enable	[0] = 0, EMSR disable for normal SDRAM. [0] = 1, EMSR enable for mobile SDRAM.	R/W	0

11.2.5.7 [010Ch] SDRAM Controller Software Reset Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SDRAM controller software reset

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_000
0	SDRAM controller software reset	Set the bit to 1 for reset the SDRAM controller	R/W	0

11.2.6 HOST Memory Configuration Register

11.2.6.1 [0140h] Host Memory Access Configuration and Status Register

15	14	13	12	11	10	9	8
Host memory interface reset	Reserved	Host memory interface ready status	Host memory interface busy status	Destination write translation to 8bpp bit select		Write rotation select	
7	6	5	4	3	2	1	0
Packed pixel 16bpp enable	Host packed write bit expansion disable	Host packed pixel select		Host rotate 0 and 180 line buffer bypass enable	Memory read/write select	Memory access type select	

Bit	Name	Description	R/W	Reset Value
15	Host memory interface reset	[15] = 1, Set the bit to 1 for reset the host interface.	R/W	0
14	Reserved	System reserved	R	0
13	Host memory interface ready status	[13] = 0, host memory interface is busy。 [13] = 1, host memory interface is idle。	R/W	0
12	Host memory interface busy status	[12] = 0, HOST memory interface is idle. [12] = 1, HOST memory interface is busy.	R/W	0
11:10	Destination write translation to 8bpp bit select	[11:10] = 00: Select databus[15:8] for image data. [11:10] = 01: Select databus[7:0] for image data. [11:10] = 10: RGB to 256 gray	R/W	00

Bit	Name	Description	R/W	Reset Value
9:8	Write rotation select	REG0140h [9:8] / Write Rotation: 00 → 0°; 01 → 90°; 10 → 180°; 11 → 270°	R/W	00
7	Packed pixel 16bpp enable	[7] = 1, Enable 16bpp transfer base on [11:10] setting.	R/W	0
6	Host packed write bit expansion disable	[6] = 1, Expansion diable. [6] = 0, Expansion enable.	R/W	0
5:4	Host packed pixel select	When the big endian(REG0020h[1] =1) and raw access will be set, the [5:4] must be set to 11. REG0140h [5:4] / Packed Pixel Mode: 00 → 2bpp; 01 → 3bpp; 10 → 4bpp; 11 → 1byte per pixel	R/W	00
3	Host rotate 0 and 180 line buffer bypass enable	[3] = 0, Enable line buffer [3] = 1, Bypass line buffer	R/W	0
2	Memory read/write select	[2] = 0, host memory interface write memory. [2] = 1, host memory interface read memory.	R/W	0
1:0	Memory access type select	[1:0] / Memory Access Type: 00 → Packed Pixel Access(Write Only); 01 → Raw Memory Access(Read/Write)	R/W	00

11.2.6.2 [0142h] Host Memory Access Triggers Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						Host transfer stop trigger	Host transfer Start trigger

Bit	Name	Description	R/W	Reset Value
15:2	Reserved	System reserved	R	0000_0000_0000_00
1	Host transfer stop trigger	[1] = 1, Stop the host interface transfer.	R/W	0
0	Host transfer start trigger	[0] = 1, Start the host interface transfer.	R/W	0

11.2.6.3 [0144h] Host Raw Memory Access Address Register 0

15	14	13	12	11	10	9	8
Host raw memory access address							
7	6	5	4	3	2	1	0
Host raw memory access address							

Bit	Name	Description	R/W	Reset Value
15:0	Host raw memory access address	Host memory access address[15:0] for raw mode.	R/W	0000_0000_ 0000_0000

11.2.6.4 [0146H] Host Raw Memory Access Address Register 1

15	14	13	12	11	10	9	8
Reserved						Host raw memory access address	
7	6	5	4	3	2	1	0
Host raw memory access address							

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9:0	Host raw memory access address	Host memory access address[25:16] for raw mode.(REG140[1:0] = 01)	R/W	0000_0000_00

11.2.6.5 [0148h] Host Raw Memory Access Count Register 0

15	14	13	12	11	10	9	8
Host raw memory access count							
7	6	5	4	3	2	1	0
Host raw memory access count							

Bit	Name	Description	R/W	Reset Value
15:0	Host raw memory access count	Host memory access count[15:0] for raw mode.	R/W	0000_0000_ 0000_0000

11.2.6.6 [014Ah] Host Raw Memory Access Count Register 1

15	14	13	12	11	10	9	8
Reserved						Host raw memory access count	
7	6	5	4	3	2	1	0
Host raw memory access count							

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9:0	Host raw memory access count	Host memory access count[25:16] for raw mode.	R/W	0000_0000_00

11.2.6.7 [014Ch] Packed Pixel Rectangular X-Start Register

15	14	13	12	11	10	9	8
Reserved				Packed pixel rectangular x-start position			
7	6	5	4	3	2	1	0
Packed pixel rectangular x-start position							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	Packed pixel rectangular x-start position	X-start position on packed pixel mode When the rotation is 0 or 180, the [11:0] must be less than line data length. When the rotation is 90 and 270, the [11:0] must be less than fram data length. The [11:0] must be divisible by 2 pixels for 1bpp.	R/W	0000_0000_0000

11.2.6.8 [014Eh] Packed Pixel Rectangular Y-Start Register

15	14	13	12	11	10	9	8
Reserved				Packed pixel rectangular y-start position			
7	6	5	4	3	2	1	0
Packed pixel rectangular y-start position							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	Packed pixel rectangular y-start position	Y-start position on packed pixel mode When the rotation is 0 or 180, the [11:0] must be less than frame data length. When the rotation is 90 and 270, the [11:0] must be less than line data length.	R/W	0000_0000_0000

11.2.6.9 [0150h] Packed Pixel Rectangular Width Register

15	14	13	12	11	10	9	8
Reserved				Packed pixel rectangular width position			
7	6	5	4	3	2	1	0
Packed pixel rectangular width							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	Packed pixel rectangular width position	When the rotaiton is 0 or 180 Packed Pixel: [11:0] 2bpp: must be divisible by 8 pixels 3bpp: must be divisible by 4 pixels 4bpp: must be divisible by 4 pixels 8bpp: must be divisible by 2 pixels	R/W	0000_0000_0000

11.2.6.10 [0152h] Packed Pixel Rectangular Height Register

15	14	13	12	11	10	9	8
Reserved			Packed pixel rectangular height position				
7	6	5	4	3	2	1	0
Packed Pixel Rectangular height bits 7-0							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	Packed pixel rectangular height position	When the rotaiton is 90 or 270 Packed Pixel: [11:0] 2bpp: must be divisible by 8 pixels 3bpp: must be divisible by 4 pixels 4bpp: must be divisible by 4 pixels 8bpp: must be divisible by 2 pixels	R/W	0000_0000_0000

11.2.6.11 [0154h] Host Memory Access Port Register

15	14	13	12	11	10	9	8
Host memory access port bits 15-8							
7	6	5	4	3	2	1	0
Host memory access port bits 7:0							

Bit	Name	Description	R/W	Reset Value
15:0	Host memory access port	Host memory access register	R/W	0000_0000_

Bit	Name	Description	R/W	Reset Value
				0000_0000

11.2.6.12 [0158h] Host Raw Memory FIFO Level Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			Host raw memory fifo level bits [3:0]				

Bit	Name	Description	R/W	Reset Value
15:5	Reserved	System reserved	R	0000_0000_000
4:0	Host raw memory fifo level	16 bit FIFO level register	R/W	0000_0

11.2.6.13 [0164h] RGB Format Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							RGB Format

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_000
0	RGB Format	[0] = 0, Input image is RGB555. [0] = 1, Input image is RGB565.	R/W	0

11.2.6.14 [01A0h] Overlap Arithmetic Configuration Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Overlap arithmetic select

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_000
0	Overlap arithmetic select	[0] = 0: Keep the first image. [0] = 1: Keep the change image.	R/W	0

11.2.7 SPI Flash Configuration Register

11.2.7.1 [0200h] SPI Flash Read Data

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
SPI flash read data							

Bits 7-0 指示從 SPI FLASH 中讀取的 8 bit 數據。

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7:0	SPI flash read data	SPI Flash read data register	R/W	0000_0000

11.2.7.2 [0202h] SPI Flash Data Output Enable

15	14	13	12	11	10	9	8
Reserved							SPI flash data output enable
7	6	5	4	3	2	1	0
SPI flash write data							

Bit	Name	Description	R/W	Reset Value
15:9	Reserved	System reserved	R	0000_000
8	SPI flash data output enable	[8] = 0, Read data from SPI flash [8] = 1, Write data from SPI flash	R/W	0
7:0	SPI flash write data	SPI Flash write data	R/W	0000_0000

11.2.7.3 [0204h] SPI Flash Chip Select Control Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
SPI flash access mode Select	SPI flash read command select	SPI flash clock divide select			SPI flash clock phase and polarity select		SPI flash enable

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7	SPI flash	Select host interface or display engine access SPI flash.	R/W	1

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td></td><td>access mode select</td><td>[7] = 1, Display engine access SPI flash
[7] = 0, Host interface access SPI flash</td><td></td><td></td></tr>
<tr><td>6</td><td>SPI flash read command select</td><td>Selec fast read or normal read for SPI flash
[6] = 0, Normal read for SPI flash
[6] = 1, Fast read for SPI flash</td><td>R/W</td><td>0</td></tr>
<tr><td>5:3</td><td>SPI flash clock divide select</td><td><table><tr><th>[5:3]</th><th>SPI Flash Clock Divide Ratio</th></tr><tr><td>000b</td><td>2:1</td></tr><tr><td>001b</td><td>3:1</td></tr><tr><td>010b</td><td>4:1</td></tr><tr><td>011b</td><td>5:1</td></tr><tr><td>100b</td><td>6:1</td></tr><tr><td>101b</td><td>7:1</td></tr><tr><td>110b</td><td>8:1</td></tr><tr><td>111b</td><td>9:1</td></tr></table></td><td>R/W</td><td>011</td></tr>
<tr><td>2:1</td><td>SPI flash clock phase and polarity select</td><td><table><tr><th>[2:1]</th><th>Valid Data</th><th>Clock Idling Status</th></tr><tr><td>00</td><td>Rising edge of SPI Flash Clock</td><td>Low</td></tr><tr><td>01</td><td>Falling edge of SPI Flash Clock</td><td>High</td></tr><tr><td>10</td><td>Falling edge of SPI Flash Clock</td><td>Low</td></tr><tr><td>11</td><td>Rising edge of SPI Flash Clock</td><td>High</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>0</td><td>SPI flash enable</td><td>[0] = 1, enable SPI flash controller.
[0] = 0, disalbe SPI flash controller.</td><td>R/W</td><td>1</td></tr>
</table>

11.2.7.4 [0206h] SPI Flash Chip Select Control Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				SPI flash busy flag	SPI flash write data register empty flag	SPI flash read data overrun flag	SPI flash read data ready flag

Bit	Name	Description	R/W	Reset Value
15:4	Reserved	System reserved	R	0000_0000_0000
3	SPI flash busy flag	[3] = 0, SPI interface idle. [3] = 1, SPI interface busy.	R/W	1

Bit	Name	Description	R/W	Reset Value
2	SPI flash write data register empty flag	[2] = 0, SPI write register is not empty. [2] = 1, SPI write register is empty.	R/W	0
1	SPI flash read data overrun flag	[1] = 0, Overrun don't occurred. [1] = 1, Overrun occurred.	R/W	0
0	SPI flash read data ready flag	[0] = 0, SPI Flash read data is vaild. [1] = 1, SPI Flash read data is available.	R/W	0

11.2.7.5 [0208h] SPI Flash Chip Select Control Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SPI flash chip select enable

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_000
0	SPI flash chip select enable	[0] = 0, Disable SPI flash CS. [0] = 1, Enable SPI flash CS.	R/W	0

11.2.8 I2C Configuration Register

11.2.8.1 [0210h] I2C Thermal Sensor Configuration Register

15	14	13	12	11	10	9	8
Reserved					I2C thermal sensor ID address		
7	6	5	4	3	2	1	0
I2C select							I2C disable

Bit	Name	Description	R/W	Reset Value
15:11	Reserved	System reserved	R	0000_0
10:8	I2C thermal sensor ID address	I2C ID address [2:0]	R/W	000
7	I2C select	I2C select enable	R/W	0
6:1	Reserved	System reserved	R	0000_00
0	I2C disable	I2C select disable	R/W	0

11.2.8.2 [0212h] I2C Thermal Sensor Status Register

15	14	13	12	11	10	9	8

Rxack status	Reserved	AI status	Reserved			Tip status	Irq_flag status
7	6	5	4	3	2	1	0
Reserved		I2C SDA pin status	I2C SCL pin status	Reserved		I2C thermal sensor ID status	I2C thermal sensor busy status

Bit	Name	Description	R/W	Reset Value
15	Rxack status	Rxack status	R	0
14	Reserved	System reserved	R	0
13	AI status	AI status	R	0
12:10	Reserved	System reserved	R	000
9	Tip status	Tip status	R	0
8	Irq_flag status	Irq status	R	0
7:6	Reserved	System reserved	R	00
5	I2C SDA pin status	[5] = 0, SDA pin is low. [5] = 1, SDA pin is high.	R	1
4	I2C SCL pin status	[4] = 0, SCL pin is low. [4] = 1, SCL pin is high.	R	1
3:2	Reserved	System reserved	R	00
1	I2C thermal sensor ID status	[1] = 0, ID has been transferred. [1] = 1, ID has not been transferred.	R	0
0	I2C thermal sensor busy status	[0] = 0, I2C is idle. [0] = 1, I2C is busy.	R	0

11.2.8.3 [0214h] I2C Thermal Sensor Read Trigger Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Start trigger	Stop trigger	Receive data trigger	Send data trigger	Ack trigger	Iack trigger	Reserved	Read trigger

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7	Start trigger	I2C start trigger	W	0
6	Stop trigger	I2C stop trigger	W	0
5	Recevice data trigger	I2C recevice data trigger	W	0
4	Send data trigger	I2C send data trigger	W	0

Bit	Name	Description	R/W	Reset Value
3	Ack trigger	I2C ack trigger	W	0
2	Iack trigger	I2C iack trigger	W	0
1	Reserved	System reserved	R	0
0	Read trigger	I2C read trigger	W	0

11.2.8.4 [0216h] I2C Thermal Sensor Temperature Value Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Temperature value							

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7:0	Temperature value	Read data for temperature data.	R	0001_1001

11.2.8.5 [0218h] I2C Transmit Value Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Transmit value							

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7:0	Transmit value	I2C write data	R/W	0000_0000

11.2.8.6 [021Ah] I2C Receive Data Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Receive data							

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7:0	Receive data	I2C receive data	R/W	0000_0000

11.2.9 Power Pin Configuration Register

11.2.9.1 [0230h] Power Pin Control Register

15	14	13	12	11	10	9	8
Reserved			PWR3 pin status	PWR2 pin status	PWR1 pin status	PWR0 pin status	PWRCOM pin status
7	6	5	4	3	2	1	0
Power cycle busy	Reserved					Power-off cycle trigger	Power-on cycle trigger

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12	PWR3 pin status	PWR3 pin status	R	0
11	PWR2 pin status	PWR2 pin status	R	0
10	PWR1 pin status	PWR1 pin status	R	0
9	PWR0 pin status	PWR0 pin status	R	0
8	PWRCOM pin status	PWRCOM pin status	R	0
7	Power cycle busy	[7] = 0, Power on/off cycle is not executed. [7] = 1, Power on/off cycle is executed.	R	0
6:2	Reserved	System reserved	R	0000_0
1	Power-off cycle trigger	Power off cycle trggier	R	0
0	Power-on cycle trigger	Power on cycle trigger	R	0

11.2.9.2 [0232h] Power Pin Configuration Register

15	14	13	12	11	10	9	8
Reserved			PWR3 pin bypass enable	PWR2 pin bypass enable	PWR1 pin bypass enable	PWR0 pin bypass enable	PWRCOM pin bypass enable
7	6	5	4	3	2	1	0
Reserved			PWR3 pin bypass value	PWR2 pin bypass value	PWR1 pin bypass value	PWR0 pin bypass value	PWRCOM pin bypass value

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12	PWR3 pin bypass enable	[12] = 0, PWR3 disable bypass [12] = 1, PWR3 enable bypass	R/W	0

Bit	Name	Description	R/W	Reset Value
11	PWR2 pin bypass enable	[11] = 0, PWR2 disable bypass [11] = 1, PWR2 enable bypass	R/W	0
10	PWR1 pin bypass enable	[10] = 0, PWR1 disable bypass [10] = 1, PWR1 enable bypass	R/W	0
9	PWR0 pin bypass enable	[9] = 0, PWR0 disable bypass [9] = 1, PWR0 enable bypass	R/W	0
8	PWRCOM pin bypass enable	[8] = 0, PWRCOM disable bypass [8] = 1, PWRCOM enable bypass	R/W	0
7:5	Reserved	System reserved	R	000
4	PWR3 pin bypass value	[4] = 0, PWR3 output 0 [4] = 1, PWR3 output 1	R/W	0
3	PWR2 pin bypass value	[3] = 0, PWR2 output 0 [3] = 1, PWR2 output 1	R/W	0
2	PWR1 pin bypass value	[2] = 0, PWR1 output 0 [2] = 1, PWR1 output 1	R/W	0
1	PWR0 pin bypass value	[1] = 0, PWR0 output 0 [1] = 1, PWR0 output 1	R/W	0
0	PWRCOM pin bypass value	[0] = 0, PWRCOM output 0 [0] = 1, PWRCOM output 1	R/W	0

11.2.9.3 [0234h] Power0 Pin To Power1 Pin Timing Delay Register

15	14	13	12	11	10	9	8
Reserved				PWR0 to PWR1 timing delay			
7	6	5	4	3	2	1	0
PWR0 to PWR1 pin timing delay							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	PWR0 to PWR1 timing delay	Delay = (([11:0] + 1) x 16) * LineCLK	R/W	0000_0000_ 0000

11.2.9.4 [0236h] Power1 Pin To Power2 Pin Timing Delay Register

15	14	13	12	11	10	9	8
Reserved				PWR1 to PWR2 timing delay			
7	6	5	4	3	2	1	0
PWR1 to PWR2 pin timing delay							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000

Bit	Name	Description	R/W	Reset Value
11:0	PWR1 to PWR2 timing delay	Delay = (([11:0] + 1) x 16) * LineCLK	R/W	0000_0000_0000

11.2.9.5 [0238h] Power Pin Timing Delay 2-3 Register

15	14	13	12	11	10	9	8
Reserved				PWR2 to PWR3 timing delay			
7	6	5	4	3	2	1	0
PWR2 to PWR3 Pin timing delay							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	PWR2 to PWR3 timing delay	Delay = (([11:0] + 1) x 16) * LineCLK	R/W	0000_0000_0000

11.2.10 Interrupt Configuration Register

11.2.10.1 [0240h] Interrupt Raw Status register

15	14	13	12	11	10	9	8
Reserved							Dithering done interrupt raw status
7	6	5	4	3	2	1	0
SDRAM self refresh interrupt raw status	Host memory r/w FIFO error interrupt Raw Status	power management controller interrupt raw status	Reserved	GPIO interrupt raw status	SDRAM access complete interrupt raw status	Display Engine Interrupt Raw Status	SDRAM initialization complete interrupt raw status

Bit	Name	Description	R/W	Reset Value
15:9	Reserved	System reserved	R	0000_000
8	Dithering done interrupt raw status	[8] = 0, Dithering interrupt is not occurred. [8] = 1, Dithering interrupt is occurred.	R/W	0
7	SDRAM self refresh interrupt raw status	[7] = 0, SDRAM self refresh interrupt is not occurred. [7] = 1, SDRAM self refresh interrupt is occurred.	R/W	0

Bit	Name	Description	R/W	Reset Value
6	Host memory r/w FIFO error interrupt raw status	[6] = 0, The interrupt is not occurred. [6] = 1, The interrupt is occurred.	R/W	0
5	Power management controller interrupt raw status	[5] = 0, The interrupt is not occurred. [5] = 1, The interrupt is occurred.	R/W	0
4	Reserved	System reserved	R/W	0
3	GPIO iInterrupt raw status	[5] = 0, The interrupt is not occurred. [5] = 1, The interrupt is occurred.	R/W	0
2	SDRAM access complete interrupt raw status	[2] = 0, The interrupt is not occurred. [2] = 1, The interrupt is occurred.	R/W	0
1	Display engine interrupt raw status	[1] = 0, The interrupt is not occurred. [1] = 1, The interrupt is occurred.	R/W	0
0	SDRAM initialization complete interrupt raw status	[0] = 0, The interrupt is not occurred. [0] = 1, The interrupt is occurred.	R/W	0

11.2.10.2 [0242h] Interrupt Masked Status Register

15	14	13	12	11	10	9	8
Reserved							Dithering done interrupt masked status
7	6	5	4	3	2	1	0
SDRAM self refresh interrupt masked status	Host memory r/w FIFO error interrupt masked status	Power management controller interrupt masked status	Reserved	GPIO interrupt masked status	SDRAM access complete interrupt masked status	Display engine interrupt masked status	SDRAM initialization complete interrupt masked status

Bit	Name	Description	R/W	Reset Value
15:9	Reserved	System reserved	R	0000_000
8	Dithering done interrupt masked status	[8] = 0, Dithering interrupt is not occurred. [8] = 1, Dithering interrupt is occurred.	R/W	0
7	SDRAM self refresh interrupt masked status	[7] = 0, SDRAM self refresh interrupt is not occurred. [7] = 1, SDRAM self refresh interrupt is occurred.	R/W	0
6	Host memory r/w FIFO error interrupt masked status	[6] = 0, The interrupt is not occurred. [6] = 1, The interrupt is occurred.	R/W	0
5	Power management controller	[5] = 0, The interrupt is not occurred.	R/W	0

Bit	Name	Description	R/W	Reset Value
	interrupt masked status	[5] = 1, The interrupt is occurred.		
4	Reserved	System reserved	R	0
3	GPIO interrupt masked status	[5] = 0, The interrupt is not occurred. [5] = 1, The interrupt is occurred.	R/W	0
2	SDRAM access complete interrupt masked status	[2] = 0, The interrupt is not occurred. [2] = 1, The interrupt is occurred.	R/W	0
1	Display engine interrupt masked status	[1] = 0, The interrupt is not occurred. [1] = 1, The interrupt is occurred.	R/W	0
0	SDRAM initialization complete interrupt masked status	[0] = 0, The interrupt is not occurred. [0] = 1, The interrupt is occurred.	R/W	0

11.2.10.3 [0244h] Interrupt Control Register

15	14	13	12	11	10	9	8
Reserved							Dithering done interrupt enable
7	6	5	4	3	2	1	0
SDRAM self refresh enter/exit interrupt enable	Host memory read/write FIFO error interrupt enable	Power management controller interrupt enable	Reserved	GPIO interrupt enable	SDRAM access complete interrupt enable	Display engine interrupt enable	SDRAM initialization complete interrupt enable

Bit	Name	Description	R/W	Reset Value
15:9	Reserved	System reserved	R	0000_000
8	Dithering done interrupt enable	[8] = 0, Disable the interrupt. [8] = 1, Enable the interruput.	R/W	0
7	SDRAM self refresh interrupt enable	[7] = 0, Disable the interrupt. [7] = 1, Enable the interruput.	R/W	0
6	Host memory read/write FIFO error interrupt enable	[6] = 0, Disable the interrupt. [6] = 1, Enable the interruput.	R/W	0
5	Power management controller interrupt enable	[5] = 0, Disable the interrupt. [5] = 1, Enable the interruput.	R/W	0
4	Reserved	System reserved	R	0
3	GPIO interrupt enable	[3] = 0, Disable the interrupt. [3] = 1, Enable the interruput.	R/W	0
2	SDRAM access complete interrupt enable	[2] = 0, Disable the interrupt. [2] = 1, Enable the interruput.	R/W	0
1	Display engine interrupt enable	[1] = 0, Disable the interrupt. [1] = 1, Enable the interruput.	R/W	0

Bit	Name	Description	R/W	Reset Value
0	SDRAM initialization complete interrupt enable	[0] = 0, Disable the interrupt. [0] = 1, Enable the interruput.	R/W	0

11.2.11 GPIO Configuration Register

11.2.11.1 [0250h] GPIO Configuration Register

15	14	13	12	11	10	9	8
Reserved						GPIO1 pull-down enable	GPIO0 pull-down enable
7	6	5	4	3	2	1	0
Reserved						GPIO1 configuration	GPIO0 configuration

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9	GPIO1 pull-down enable	[9] =0, GPIO1 pull-down disable. [9] =1, GPIO1 pull-down enable.	R/W	0
8	GPIO0 pull-donw enable	[8] =0, GPIO0 pull-down disable. [8] =1, GPIO0 pull-down enable.	R/W	0
7:2	Reserved	System reserved	R	0000_00
1	GPIO1 configuration	[1] = 0, GPIO1 set to input [1] = 1, GPIO1 set to output	R/W	0
0	GPIO0 configuration	[0] = 0, GPIO0 set to input [0] = 1, GPIO0 set to output	R/W	0

11.2.11.2 [0252h] GPIO Status/Control Register

15	14	13	12	11	10	9	8
Reserved						GPIO1 input status	GPIO0 input status
7	6	5	4	3	2	1	0
Reserved						GPIO1 data output control	GPIO0 data output control

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9	GPIO1 input status	[9] =0, GPIO1 input is low. [9] =1, GPIO1 input is high.	R	0
8	GPIO0 input status	[8] =0, GPIO0 input is low	R	0

Bit	Name	Description	R/W	Reset Value
		[8] =1, GPIO0 input is high.		
7:2	Reserved	System reserved	R	0000_00
1	GPIO1 data output control	[1] = 0, GPIO1 output low. [1] = 1, GPIO1 output high	R/W	0
0	GPIO0 data output control	[0] = 0, GPIO0 output low. [0] = 1, GPIO0 output highi.	R/W	0

11.2.11.3 [0254h] GPIO Interrupt Enable Register

15	14	13	12	11	10	9	8
Reserved						GPIO1 negative edge interrupt enable	GPIO0 negative edge interrupt enable
7	6	5	4	3	2	1	0
Reserved						GPIO1 positive edge interrupt enable	GPIO0 positive edge interrupt enable

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9	GPIO1 negative edge interrupt enable	[9] =0, Disable GPIO1 negative edge interrupt. [9] =1, Enable GPIO1 negative edge interrupt.	R/W	0
8	GPIO0 negative edge interrupt enable	[8] =0, Disable GPIO0 negative edge interrupt. [8] =1, Enable GPIO0 negative edge interrupt.	R/W	0
7:2	Reserved	System reserved	R	0000_00
1	GPIO1 positive edge interrupt enable	[1] =0, Disable GPIO1 positive edge interrupt. [1] =1, Enable GPIO1 positive edge interrupt.	R/W	0
0	GPIO0 positive edge interrupt enable	[0] =0, Disable GPIO0 positive edge interrupt. [0] =1, Enable GPIO0 positive edge interrupt.	R/W	0

11.2.11.4 [0256h] GPIO Interrupt Status Register

15	14	13	12	11	10	9	8

Reserved						GPIO1 negative edge interrupt status	GPIO0 negative edge interrupt status
7	6	5	4	3	2	1	0
Reserved						GPIO1 positive edge interrupt status	GPIO0 positive edge interrupt status

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9	GPIO1 negative edge interrupt status	[9] =0, GPIO1 negative edge interrupt is not occurred. [9] =1, GPIO1 negative edge interrupt is occurred.	R/W	0
8	GPIO0 negative edge interrupt status	[8] =0, GPIO0 negative edge interrupt is not occurred. [8] =1, GPIO0 negative edge interrupt is occurred.	R/W	0
7:2	Reserved	System reserved	R	0000_00
1	GPIO1 positive edge interrupt status	[1] =0, GPIO1 positive edge interrupt is not occurred. [1] =1, GPIO1 positive edge interrupt is occurred.	R/W	0
0	GPIO0 positive edge interrupt status	[0] =0, GPIO0 positive edge interrupt is not occurred. [0] =1, GPIO0 positive edge interrupt is occurred.	R/W	0

11.2.11.5 [0258h] GPIO Sleep Mode Output Control Register

15	14	13	12	11	10	9	8
Reserved							GPIO output data changing enable for sleep mode
7	6	5	4	3	2	1	0
Reserved						GPIO1 sleep mode data output control	GPIO0 sleep mode data output control

Bit	Name	Description	R/W	Reset Value
15:9	Reserved	System reserved	R	0000_000

Bit	Name	Description	R/W	Reset Value
8	GPIO output data changing enable for sleep mode	[8] =0, Disable GPIO output changing for sleep mode [8] =1, Enable GPIO output changing for sleep mode	R/W	0
7:2	Reserved	System reserved	R	0000_00
1	GPIO1 sleep mode data output control	[1] =0, GPIO1 output low for sleep mode [1] =1, GPIO1 output high for sleep mode	R/W	0
0	GPIO0 sleep mode data output control	[0] =0, GPIO0 output low for sleep mode [0] =1, GPIO0 output high for sleep mode	R/W	0

11.2.12 Command RAM Configuration Register

11.2.12.1 [0290h] Command RAM Controller Configuration Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Command ram access read/write select

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_000
0	Command ram access read/write select	[0] = 0, Command ram write enable. [0] = 1, Command ram read enable.	R/W	0

11.2.12.2 [0292h] Command RAM Controller Address Register

15	14	13	12	11	10	9	8
Reserved					Command ram address pointer		
7	6	5	4	3	2	1	0
Command ram address pointer							

Bit	Name	Description	R/W	Reset Value
15:11	Reserved	System reserved	R	0000_0
10:0	Command ram address pointer	Command ram address pointer, when the write or read is executed, the pointer is auto incremented by 2.	R/W	0000_0000_000

11.2.12.3 [0294h] Command RAM Controller Access Port Register

15	14	13	12	11	10	9	8
Command ram access port							
7	6	5	4	3	2	1	0
Command ram access port							

Bit	Name	Description	R/W	Reset Value
15:0	Command ram access port	When the REG290h [0] is set to 0, the register is read data from command ram. When the REG290h [0] is set to 1, the register is write data for command ram.	R/W	0000_0000_ 0000_0000

11.2.13 Display Timing Configuration Register

11.2.13.1 [0300h] Frame Data Length Register

15	14	13	12	11	10	9	8
Reserved			Frame data length bits [12:8]				
7	6	5	4	3	2	1	0
Frame data length bits [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Frame data length	Frame data length	R/W	0_0010_ 0101_1000

11.2.13.2 [0302h] Frame Sync. Length Register

15	14	13	12	11	10	9	8
Reserved			Frame sync length				
7	6	5	4	3	2	1	0
Frame sync length							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Frame sync length	Frame sync length	R/W	0_0000_ 0000_0100

11.2.13.3 [0304h] Frame Begin/End Length Register

15	14	13	12	11	10	9	8

Frame end length							
7	6	5	4	3	2	1	0
Frame begin length							

Bit	Name	Description	R/W	Reset Value
15:13	Frame end length	Frame end length plus 1	R/W	0000_1010
12:0	Frame begin length	Frame begin length plus 1	R/W	0000_0100

11.2.13.4 [0306h] Line Data Length Register

15	14	13	12	11	10	9	8
Reserved			Line data length bits [12:8]				
7	6	5	4	3	2	1	0
Line data length bits [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Line data length	Line data length	R/W	0_0011_ 0010_0000

11.2.13.5 [0308h] Line Sync. Length Register

15	14	13	12	11	10	9	8
Reserved			Line sync length				
7	6	5	4	3	2	1	0
Line sync length							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Line sync length	Line sync length	R/W	0_0000_ 0000_1010

11.2.13.6 [030Ah] Line Begin/End Length Register

15	14	13	12	11	10	9	8
Line end length							
7	6	5	4	3	2	1	0
Line begin length							

Bit	Name	Description	R/W	Reset Value
15:8	Line end length	Line end length When REG030Ch [11] is set to 0, the	R/W	0110_0100

Bit	Name	Description	R/W	Reset Value
		[15:8] must be equal to or larger than 2. [15:8] = (REG030Ah[15:8] -1) * SDCLK period – Padded Data Output Time – PCLK period When REG030Ch [11] is set to 1, [15:8] must be equal to or larger than 4. [15:8] = ((REG030Ah[15:8] / 2) - 1) * SDCLK period – Padded Data Output Time – PCLK period		
7:0	Line begin length	Line begin length	R/W	0000_0100

11.2.14 Source Driver Configuration Register

11.2.14.1 [030Ch] Source Drive Configuration Register

15	14	13	12	11	10	9	8
Source driver chip enable start bits				Source driver pixel output count select	Source driver chip enable reverse	Source driver output reverse	Source driver shift
7	6	5	4	3	2	1	0
Source driver output size select bit							

Bit	Name	Description	R/W	Reset Value
15:12	Source driver chip enable start bits	[10] = 0b: 0000b: Chip0 ->Chip1 ->Chip2 0001b: Chip1 ->Chip2 ->Chip0 0010b: Chip2 ->Chip0-> Chip1 0011b ~1111b: Reserved [10] = 1b: 0000b: Chip0 ->Chip2 ->Chip1 0001b: Chip1 ->Chip0 ->Chip2 0010b: Chip2 ->Chip1 ->Chip0 0011b ~1111b: Reserved	R/W	0000
11	Source driver pixel output count select	[11] = 0, 4 pixels per source clock [11] = 1, 8 pixels per source clock	R/W	0
10	Source driver chip enable reverse	[10] = 0, the source driver chip enable sequence is not reversed. [10] = 1, the source driver chip enable sequence is reversed.	R/W	0

Bit	Name	Description	R/W	Reset Value
9	Source driver output reverse	<table><tr><th>[11]</th><th>[9]</th><th>Parallel Output to Source Driver</th></tr><tr><td>0</td><td>0</td><td>P3,P2,P1,P0</td></tr><tr><td>0</td><td>1</td><td>P0,P1,P2,P3</td></tr><tr><td>1</td><td>0</td><td>P7,P6,P5,P4,P3,P2,P1,P0</td></tr><tr><td>1</td><td>1</td><td>P0,P1,P2,P3,P4,P5,P6,P7</td></tr></table>	R/W	0
8	Source driver shift	[8] = 0, the data is shifted from left to rigtht. [8] = 1, the data is shifted from right to left.	R/W	0
7:0	Source driver output size select bit	REG030Ch [7:0] = value in pixels / 4	R/W	0110_0100

11.2.14.2 [030Eh] Source Drive Configuration Register

15	14	13	12	11	10	9	8
Source driver SDOED delay					Source driver double data rate enable	source driver swap padding pixels	source driver early SDOE assert disable
7	6	5	4	3	2	1	0
Reserved						Gate driver right/left select	Gate driver start pulse polarity

Bit	Name	Description	R/W	Reset Value
15:11	Source driver SDOED delay	When REG030Ch [11] is set to 1, the delay from SDLE to SDOED is valid.	R/W	0000_0
10	Source driver double data rate enable	Source driver double data rate enable	R/W	0
9	Source driver swap padding pixels	Source driver swap padding pixels	R/W	0
8	Source driver early SDOE assert disable	[8] = 0, Enable assert SDOE before SDLE. [8] = 1, Disable assert SDOE before SDLE	R/W	0
7:2	Reserved	System reserved	R	0000_00
1	Gate driver right/left select	[1] = 0, GDRL output low. [1] = 1, GDRL output high.	R/W	0
0	Gate driver start pulse polarity	[0] = 0, Start pulse is negative edge. [0] = 1, Start pulse is positive edge.	R/W	0

11.2.15 Display Buffer Configuration Register

11.2.15.1 [0310h] Image Buffer Start Register 0

15	14	13	12	11	10	9	8
Image buffer start address							
7	6	5	4	3	2	1	0
Image buffer start address							

Bit	Name	Description	R/W	Reset Value
15:0	Image buffer start address	Image buffer start address[15:0]	R/W	0000_0000_ 0000_0000

11.2.15.2 [0312h] Image Buffer Start Register 1

15	14	13	12	11	10	9	8
Reserved						Image buffer start address bit [25:24]	
7	6	5	4	3	2	1	0
Image buffer start address bit [23:16]							

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9:0	Image buffer start address	Image buffer start address[25:16]	R/W	00_0000_0000

11.2.15.3 [0314h] Update Buffer Start Register 0

15	14	13	12	11	10	9	8
Update buffer start address							
7	6	5	4	3	2	1	0
Update buffer start address							

Bit	Name	Description	R/W	Reset Value
15:0	Update buffer start address	Update buffer start address[15:0]	R/W	0000_0000_ 0000_0000

11.2.15.4 [0316h] Update Buffer Start Register 1

15	14	13	12	11	10	9	8
Reserved						Update buffer start address bit [25:24]	
7	6	5	4	3	2	1	0

Update buffer start address bits [23:16]

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	0000_00
9:0	Update buffer start address	Update image buffer start address[25:16]	R/W	00_0000_0000

11.2.16 General Configuration Register

11.2.16.1 [0320h] Temperature Device Select Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Temperature auto retrieval disable

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_ 0000_000
0	Temperature auto retrieval disable	[0] = 0, Enable temperature auto retrieval [0] = 1, Disable temperature auto retrieval	R/W	0

11.2.16.2 [0322h] Temperature Value Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Temperature value register							

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7:0	Temperature value register	Temperature value for waveform select and display.	R/W	0000_0000

11.2.16.3 [032Ch] General Configuration Register

15	14	13	12	11	10	9	8
Reserved					Area coordinate	Area coordinate rotation	

					end size select	select bits [1:0]	
7	6	5	4	3	2	1	0
Reserved							

Bit	Name	Description	R/W	Reset Value
15:11	Reserved	System reserved	R	0000_0
10	Area coordinate end size select	[10]= 0, REG[0344h] ~ REG[0346h] are X/Y end point. [10]=1, REG[0344h] ~ REG[0346h] are width/height.	R/W	0
9:8	Area coordinate rotation select bits	[9:8] / Rotation Mode 00 / 0° 01 / 90° 10 / 180° 11 / 270°	R/W	00
7:0	Reserved	System reserved	R	0000_0000

11.2.16.4 [032Eh] LUT Mask Register

15	14	13	12	11	10	9	8
LUT 15 MASK	LUT 14 MASK	LUT 13 MASK	LUT 12 MASK	LUT 11 MASK	LUT 10 MASK	LUT 9 MASK	LUT 8 MASK
7	6	5	4	3	2	1	0
LUT 7 MASK	LUT 6 MASK	LUT 5 MASK	LUT 4 MASK	LUT 3 MASK	LUT 2 MASK	LUT 1 MASK	LUT 0 MASK

Bit	Name	Description	R/W	Reset Value
15:0	LUT x MASK	[x] = 0, Masked LUT [x] = 1, Unmasked LUT	R/W	0000_0000_0000_0000

11.2.17 Update Buffer Configuration Register

11.2.17.1 [0330h] Update Buffer Configuration Register

15	14	13	12	11	10	9	8
DSPE soft reset	Reserved			Last waveform mode			
7	6	5	4	3	2	1	0
LUT auto select enable	Reserved				LUT index format select		

Bit	Name	Description	R/W	Reset Value
15	DSPE soft reset	[15] = 1, Reset DSPE by software.	R/W	0
14:12	Reserved	System reserved	R	000
11:8	Last waveform mode	Last waveform mode of display	R/W	0000
7	LUT auto select enable	[7] = 0, Disable LUT auto select. [7] = 1, Enable LUT auto select.	R/W	0
6:3	Reserved	System reserved	R	000
2:0	LUT index format select	REG0330h [2:0] / LUT Index Format 000 / P2N 001 / N/A 010 / P3N 011 / N/A 100 / P4N 101 / N/A 110 / N/A 111 / N/A	R/W	00

11.2.17.2 [0332h] Update Buffer Pixel Set Value Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Update buffer pixel set value							

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7:0	Update buffer pixel set value	Update buffer pixel set value.	R/W	0000_0000

11.2.17.3 [0334h] Display Engine Control/Trigger Register

15	14	13	12	11	10	9	8
Reserved		Update rectangle mode		Display update waveform mode			
7	6	5	4	3	2	1	0
Display update LUT select bits				Operation mode select			Operation trigger

Bit	Name	Description	R/W	Reset Value
15:14	Reserved	System reserved	R	00

Bit	Name	Description	R/W	Reset Value
13:12	Update rectangle mode	[13:12] Update Rectangle Mode 00 Full Display Size Update 01 Host X/Y Start/End positions are used (see REG[0348h] ~ REG [0346h]) 10 X/Y Start/End positions are specified by REG[0340h] ~ REG[0346h]) 11 Reserved	R/W	00
11:8	Display update waveform mode	Display update waveform mode.	R/W	0000
7:4	Display update LUT select bits	When REG[0330h] bit 7 is set to 1, LUT will be auto selected.	R/W	0000
3:1	Operation mode select	[3:1] Operation Mode 000 Waveform Header Read 001 Update Buffer Set Value Refresh 010 Update Buffer Image Buffer Refresh 011 Full Display Update 100 Partial Display Update 101 Gate Driver Clear Operation 110 ~ 111 Reserved	R/W	000
0	Operation trigger	Display trigger.	W	0

11.2.18 LUT Status Register

11.2.18.1 [0336h] LUT STATUS Register 0

15	14	13	12	11	10	9	8
LUT 15 update busy	LUT 14 update busy	LUT 13 update busy	LUT 12 update busy	LUT 11 update busy	LUT 10 update busy	LUT 9 update busy	LUT 8 update busy
7	6	5	4	3	2	1	0
LUT 7 update busy	LUT 6 update busy	LUT 5 update busy	LUT 4 update busy	LUT 3 update busy	LUT 2 update busy	LUT 1 update busy	LUT 0 update busy

Bit	Name	Description	R/W	Reset Value

Bit	Name	Description	R/W	Reset Value
15:0	LUT x update busy	[x] = 0, LUT is idle. [x] = 1, LUT is busy.	R/W	0000_0000_ 0000_0000

11.2.18.2 [0338h] Display Engine Busy Status Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	Masked LUT available status	LUT available status	Reserved	Display frame busy	Update buffer refresh status	Frame memory access busy	Operation trigger busy

Bit	Name	Description	R/W	Reset Value
15:7	Reserved	System reserved	R	0000_0000
6	Masked LUT available status	[6] = 0, Mask LUT is not available. [6] = 1, Mask LUT is available.	R/W	0
5	LUT available status	[5] = 0, All LUT is not available. [5] = 1, one or more LUTs are available.	R/W	0
4	Reserved	System reserved	R	0
3	Display frame busy	[3] = 0, Dislay is done. [3] = 1, Display is running.	R/W	0
2	Update buffer refresh status	[2] = 0, update buffer is idle. [2] = 1, update buffer is busy.	R/W	0
1	Frame memory access busy	[1] = 0, Frame memory is idle.. [1] = 1, Frame memory is busy.	R/W	0
0	Operation trigger busy	[0] = 0, Operation trigger is idle. [0] = 1, Operation trigger is busy.	R/W	0

11.2.19 Interrupt Register

11.2.19.1 [033Ah] Display Engine Interrupt Raw Status Register

15	14	13	12	11	10	9	8
Reserved		Image buffer update incomplete interrupt raw status	Reserved		Temperature out of range interrupt raw status	LUT request error interrupt raw status	Operation trigger error interrupt raw status
7	6	5	4	3	2	1	0
LUT area overlap	Display pipe FIFO	All frames complete	Update buffer changed	One LUT N-frame	Display output frame complete	Update buffer	Operation trigger done

conflict interrupt raw status	underflow interrupt raw status	interrupt raw status	interrupt raw status	display complete interrupt raw status	interrupt raw status	refresh done interrupt raw status	interrupt raw status

Bit	Name	Description	R/W	Reset Value
15:14	Reserved	System reserved	R	00
13	Image buffer update incomplete interrupt raw status	[13] = 0, Image buffer update imcomplete interrupt is not occurred. [13] = 1, Image buffer update imcomplete interrupt is occurred.	R/W	0
12:11	Reserved	System reserved	R	00
10	Temperature out of range interrupt raw status	[10] = 0, Temperature out of range interrupt is not occurred. [10] = 1, Temperature out of range interrupt is occurred.	R/W	0
9	LUT request error interrupt raw status	[9] = 0, LUT request error interrupt is not occurred. [9] = 1, LUT request error interrupt is occurred.	R/W	0
8	Operation trigger error interrupt raw status	[8] = 0, Operation trigger error interrupt is not occurred. [8] = 1, Operation trigger error interrupt is occurred.	R/W	0
7	LUT area overlap conflict interrupt raw status	[7] = 0, LUT area overlap conflict interrupt is not occurred. [7] = 1, LUT area overlap conflict interrupt is occurred.	R/W	0
6	Display pipe FIFO underflow interrupt raw status	[6] = 0, Display pipe FIFO underflow interrupt is not occurred. [6] =1, Display pipe FIFO underflow interrupt is occurred.	R/W	0
5	All frames complete interrupt raw status	[5] = 0, All frames complete interrupt is not occurred. [5] = 1, All frames complete interrupt is occurred.	R/W	0
4	Update buffer changed interrupt raw status	[4] = 0, Update buffer changed interrupt is not occurred. [4] = 1, Update buffer changed interrupt is occurred.	R/W	0
3	One LUT N-frame display complete interrupt raw status	[3] = 0, One LUT N-frame display complete interrupt is not occurred.	R/W	0

Bit	Name	Description	R/W	Reset Value
		[3] = 1, One LUT N-frame display complete interrupt is occurred.		
2	Display output frame complete interrupt raw status	[2] = 0, Display output frame complete interrupt is not occurred. [2] = 1, Display output frame complete interrupt is occurred.	R/W	0
1	Update buffer refresh done interrupt raw status	[1] = 0, Update buffer refresh done interrupt is not occurred. [1] = 1, Update buffer refresh done interrupt is occurred.	R/W	0
0	Operation trigger done interrupt raw status	[0] = 0, Operation trigger done interrupt is not occurred. [0] = 1, Operation trigger done interrupt is occurred.	R/W	0

11.2.19.2 [033Ch] Display Engine Interrupt Masked Status Register

15	14	13	12	11	10	9	8
Reserved		Image buffer update incomplete interrupt masked status	Reserved		Temperature out of range interrupt masked status	LUT request error interrupt masked status	Operation trigger error interrupt masked status
7	6	5	4	3	2	1	0
LUT area overlap conflict interrupt masked status	Display pipe FIFO underflow interrupt masked status	All frames complete interrupt masked status	Update buffer changed interrupt masked status	One LUT N-frame display complete interrupt masked status	Display output frame Complete interrupt masked status	Update buffer refresh done interrupt masked status	Operation trigger done interrupt masked status

Bit	Name	Description	R/W	Reset Value
15:14	Reserved	System reserved	R	00
13	Image buffer update incomplete interrupt mask status	[13] = 0, Image buffer update imcomplete interrupt is not occurred. [13] = 1, Image buffer update imcomplete interrupt is occurred.	R/W	0
12:11	Reserved	System reserved	R	00
10	Temperature out of range interrupt mask status	[10] = 0, Temperature out of range interrupt is not occurred.	R/W	0

Bit	Name	Description	R/W	Reset Value
		[10] = 1, Temperature out of range interrupt is occurred.		
9	LUT request error interrupt mask status	[9] = 0, LUT request error interrupt is not occurred. [9] = 1, LUT request error interrupt is occurred.	R/W	0
8	Operation trigger error interrupt mask status	[8] = 0, Operation trigger error interrupt is not occurred. [8] = 1, Operation trigger error interrupt is occurred.	R/W	0
7	LUT area overlap conflict interrupt mask status	[7] = 0, LUT area overlap conflict interrupt is not occurred. [7] = 1, LUT area overlap conflict interrupt is occurred.	R/W	0
6	Display pipe FIFO underflow interrupt mask status	[6] = 0, Display pipe FIFO underflow interrupt is not occurred. [6] =1, Display pipe FIFO underflow interrupt is occurred.	R/W	0
5	All frames complete interrupt mask status	[5] = 0, All frames complete interrupt is not occurred. [5] = 1, All frames complete interrupt is occurred.	R/W	0
4	Update buffer changed interrupt mask status	[4] = 0, Update buffer changed interrupt is not occurred. [4] = 1, Update buffer changed interrupt is occurred.	R/W	0
3	One LUT N-frame display complete interrupt mask status	[3] = 0, One LUT N-frame display complete interrupt is not occurred. [3] = 1, One LUT N-frame display complete interrupt is occurred.	R/W	0
2	Display output frame complete interrupt mask status	[2] = 0, Display output frame complete interrupt is not occurred. [2] = 1, Display output frame complete interrupt is occurred.	R/W	0
1	Update buffer refresh done interrupt mask status	[1] = 0, Update buffer refresh done interrupt is not occurred. [1] = 1, Update buffer refresh done interrupt is occurred.	R/W	0
0	Operation trigger done interrupt mask status	[0] = 0, Operation trigger done interrupt is not occurred. [0] = 1, Operation trigger done interrupt is occurred.	R/W	0

11.2.19.3 [033Eh] Display Engine Interrupt Enable Register

15	14	13	12	11	10	9	8
Reserved		Image buffer update incomplete interrupt enable	Reserved		Temperature out of range interrupt enable	LUT request error interrupt enable	Operation trigger error interrupt enable
7	6	5	4	3	2	1	0
LUT area overlap conflict interrupt enable	Display pipe FIFO underflow interrupt enable	All frames complete interrupt enable	Update buffer changed interrupt enable	One LUT N-frame display complete interrupt enable	Display output 1 frame complete interrupt enable	Update buffer refresh done interrupt enable	Operation trigger done interrupt enable

Bit	Name	Description	R/W	Reset Value
15:14	Reserved	System reserved	R	00
13	Image buffer update incomplete interrupt enable	[13] = 0, Disable image buffer update incomplete interruput [13] = 1, Enable image buffer update incomplete interrupt.	R/W	0
12:11	Reserved	System reserved	R	00
10	Temperature out of range interrupt enable	[10] = 0, Disable temperature out of range interrupt [10] = 1, Enable temperature out of range interrupt.	R/W	0
9	LUT request error interrupt enable	[9] = 0, Disable LUT request error interrupt. [9] = 1, Enable LUT request error interrupt.	R/W	0
8	Operation trigger error interrupt enable	[8] = 0, Disable operation trigger error interrupt. [8] = 1, Enable operation trigger error interrupt.	R/W	0
7	LUT area overlap conflict interrupt enable	[7] = 0, Disable LUT area overlap conflict interrupt. [7] = 1, Enable LUT area ovelap conflict interrupt.	R/W	0
6	Display pipe FIFO underflow interrupt enable	[6] = 0, Disable pipe FIFO underflow interrupt. [6] = 1, Enable pipe FIFO underflow interrupt.	R/W	0

Bit	Name	Description	R/W	Reset Value
5	All frames complete interrupt enable	[5] = 0, Disable all frames complete interrupt. [5] = 1, Enable all frames complete interrupt	R/W	0
4	Update buffer changed interrupt enable	[4] = 0, Disable update buffer changed interrupt. [4] = 1, Enable update buffer changed interrupt.	R/W	0
3	One LUT N-frame display complete interrupt enable	[3] = 0, Disable one LUT display complete interrupt. [3] = 1, Enable one LUT display complete interrupt.	R/W	0
2	Display output frame complete interrupt enable	[2] = 0, Disable display complete interrupt [2] = 1, Enable display complete interrupt	R/W	0
1	Update Buffer Refresh Done Interrupt Enable	[1] = 0, Disable update buffer refresh done interrupt. [1] = 1, Enable update buffer refresh done interrupt.	R/W	0
0	Operation trigger done interrupt enable	[0] = 0, Disable operation trigger done interrupt. [0] = 1, Enable operation trigger done interrupt.	R/W	0

11.2.20 Display Engine Configuration Register

11.2.20.1 [0340h] Area Update Pixel Rectangular X-Start Register

15	14	13	12	11	10	9	8
Reserved				Area update pixel rectangular x-start[11:8]			
7	6	5	4	3	2	1	0
Area update pixel rectangular x-start[7:0]							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	Area update pixel rectangular x-start	Area update pixel rectangular x-start	R/W	0000_0000_0000

11.2.20.2 [0342h] Area Update Pixel Rectangular Y-Start Register

15	14	13	12	11	10	9	8

Reserved				Area update pixel rectangular y-start[11:8]			
7	6	5	4	3	2	1	0
Area update pixel rectangular y-start[7:0]							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	Area update pixel rectangular y-start	Area update pixel rectangular y-start	R/W	0000_0000_ 0000

11.2.20.3 [0344h] Area Update Pixel Rectangular X-End Position/Horizontal Size

15	14	13	12	11	10	9	8
Reserved			Area update pixel rectangular x-end position/horizontal size				
7	6	5	4	3	2	1	0
Area update pixel rectangular x-end position/horizontal size							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Area update pixel rectangular x-end position/horizontal size	Area update pixel rectangular x-end position/horizontal size	R/W	0_0000_ 0000_0000

11.2.20.4 [0346h] Area Update Pixel Rectangular Y-End Position/Vertical Size

15	14	13	12	11	10	9	8
Reserved			Area update pixel rectangular y-end position/vertical size				
7	6	5	4	3	2	1	0
Area update pixel rectangular y-end position							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Area update pixel rectangular y-end position/vertical size	Area update pixel rectangular y-end position/vertical size	R/W	0_0000_ 0000_0000

11.2.20.5 [0348h] Host Pixel Rectangular X-start Position

15	14	13	12	11	10	9	8
Reserved			Host pixel rectangular x-start position				
7	6	5	4	3	2	1	0
Host pixel rectangular X-start position							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000

Bit	Name	Description	R/W	Reset Value
12:0	Host pixel rectangular x-start position	Host pixel rectangular x-start position	R/W	0_0000_ 0000_0000

11.2.20.6 [034Ah] Host Pixel Rectangular Y-start Position

15	14	13	12	11	10	9	8
Reserved			Host pixel rectangular y-start position				
7	6	5	4	3	2	1	0
Host pixel rectangular y-start position							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Host pixel rectangular y-start position	Host pixel rectangular y-start position	R/W	0_0000_ 0000_0000

11.2.20.7 [034Ch] Host Pixel Rectangular X-end Position

15	14	13	12	11	10	9	8
Reserved			Host pixel rectangular x-end position				
7	6	5	4	3	2	1	0
Host pixel rectangular x-end position							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Host pixel rectangular x-end position	Host pixel rectangular x-end position	R/W	0_0000_ 0000_0000

11.2.20.8 [034Eh] Host Pixel Rectangular Y-End Position

15	14	13	12	11	10	9	8
Reserved			Host pixel rectangular y-end position				
7	6	5	4	3	2	1	0
Host pixel rectangular y-end position							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Host pixel rectangular y-end position	Host pixel rectangular y-end position	R/W	0_0000_ 0000_0000

11.2.21 SPI Flash Start Address Configuration Register

11.2.21.1 [0350h] Waveform Header Serial Flash Waveform Register 0

15	14	13	12	11	10	9	8
Waveform header serial flash address							
7	6	5	4	3	2	1	0
Waveform header serial flash address							

Bit	Name	Description	R/W	Reset Value
15:0	Waveform header serial flash address	Waveform start address [15:0]	R/W	0000_0000_0000_0000

11.2.21.2 [0352h] Waveform Header Serial Flash Waveform Register 1

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Waveform header serial flash address bit [23:16]							

Bit	Name	Description	R/W	Reset Value
15:8	Reserved	System reserved	R	0000_0000
7:0	Waveform header serial flash address	Waveform start address [23:16]	R/W	0000_0000

11.2.22 Advanced Display Configuration Register

11.2.22.1 [0370h] Source Driver Advanced Timing Configuration Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					SDLE enable polarity	SDOE full frame drive enable	SDOE early assert on SDLE enable

Bit	Name	Description	R/W	Reset Value
15:3	Reserved	System reserved	R	0000_0000_0000_0
2	SDLE enable polarity	[2] = 0, SDLE is positive edge [2] = 1, SDLE is negative edge	R/W	0

Bit	Name	Description	R/W	Reset Value
1	SDOE full frame drive enable	[1] = 0, SDOE line enable [1] = 1, SDOE frame enable	R/W	0
0	SDOE early assert on SDLE enable	[0] = 0, SDOE valid after SDLE [0] = 1, SDOE valid before SDLE	R/W	0

11.2.22.2 [0372h] Gate Driver Advanced Timing Configuration Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					GDCLK polarity	GDOE toggle with GDCLK enable	GDCLK valid time after SDLE enable

Bit	Name	Description	R/W	Reset Value
15:3	Reserved	System reserved	R	0000_0000_0000_0
2	GDCLK polarity	[2] = 0, GDCLK is positive edge [2] = 1, GDCLK is negative edge	R/W	0
1	GDOE toggle with GDCLK enable	[1] = 0, GDOE frame enable [1] = 1, GDOE line enable	R/W	0
0	GDCLK valid time after SDLE enable	[0] = 0, GDCLK valid before SDLE [0] = 1, GDCLK valid after SDLE	R/W	0

11.2.23 AUO Configuration Registers

11.2.23.1 [0380h] XDIO Pulse Width Configuration Register

15	14	13	12	11	10	9	8
Reserved			XDIO pulse width [12:8]				
7	6	5	4	3	2	1	0
XDIO pulse width [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	XDIO pulse width	XDIO pulse width	R/W	0_0000_0000_0000

11.2.23.2 [0382h] LD Delay Configuration Register

15	14	13	12	11	10	9	8

Reserved			LD delay [12:8]				
7	6	5	4	3	2	1	0
LD delay [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	LD delay	Delay from XDIO to LD	R/W	0_0000_ 0000_0000

11.2.23.3 [0384h] LD Pulse Width Configuration Register

15	14	13	12	11	10	9	8
Reserved			LD pulse width [12:8]				
7	6	5	4	3	2	1	0
LD pulse width [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	LD pulse width	LD pulse width	R/W	0_0000_ 0000_0000

11.2.23.4 [0386h] YCLK Delay Configuration Register

15	14	13	12	11	10	9	8
Reserved			YCLK delay [12:8]				
7	6	5	4	3	2	1	0
YCLK delay [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	YCLK delay	Delay from XDIO to YCLK	R/W	0_0000_ 0000_0000

11.2.23.5 [0388h] YCLK Pulse Width Configuration Register

15	14	13	12	11	10	9	8
Reserved			YCLK pulse width [12:8]				
7	6	5	4	3	2	1	0
YCLK pulse width [7:0]							

Bit	Name	Description	R/W	Reset Value

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	YCLK pulse width	YCLK pulse width	R/W	0_0000_ 0000_0000

11.2.23.6 [038Ah] YOE Delay Configuration Register

15	14	13	12	11	10	9	8
Reserved			YOE delay [12:8]				
7	6	5	4	3	2	1	0
YOE delay [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	YOE delay	Delay from XDIO to YOE	R/W	0_0000_ 0000_0000

11.2.23.7 [038Ch] YOE Pulse Width Configuration Register

15	14	13	12	11	10	9	8
Reserved			YOE pulse width [12:8]				
7	6	5	4	3	2	1	0
YOE pulse width [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	YOE pulse width	YOE pulse width	R/W	0_0000_ 0000_0000

11.2.23.8 [038Eh] YDIO Delay Configuration Register

15	14	13	12	11	10	9	8
Reserved			YDIO delay [12:8]				
7	6	5	4	3	2	1	0
YDIO delay [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	YDIO delay	Delay from XDIO to YDIO	R/W	0_0000_ 0000_0000

11.2.23.9 [0390h] YDIO Pulse Width Configuration Register

15	14	13	12	11	10	9	8
Reserved			YDIO pulse width [12:8]				
7	6	5	4	3	2	1	0
YDIO pulse width [7:0]							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	YDIO pulse width	YDIO pulse width	R/W	0_0000_ 0000_0000

11.2.23.10 [0392h] AUO Enable and Polarity Control Register

15	14	13	12	11	10	9	8
Reserved							Enable AUO/LG driver
7	6	5	4	3	2	1	0
Reserved		YDIO polarity	YOE polarity	YCLK polarity	LD polarity	XDIO polarity	Disable XCLK gate

Bit	Name	Description	R/W	Reset Value
15:9	Reserved	System reserved	R	0000_000
8	Enable AUO/LG driver	[8]=0, LG model [8]=1, AUO model	R/W	0
7:6	Reserved	System reserved	R	00
5	YDIO polarity	[5] = 0,YDIO is negative edge [5] = 1,YDIO is positive edge	R/W	0
4	YOE polarity	[4] = 0，YOE is negative edge [4] = 1，YOE is positive edge	R/W	0
3	YCLK polarity	[3] = 0，YCLK negative edge [3] = 1，YCLK is positive edge	R/W	0
2	LD polarity	[2] = 0，LD is negative edge [2] = 1，LD is positive edge	R/W	0
1	XDIO polarity	[1] = 0，XDIO is negative edge [1] = 1，XDIO is positive edge	R/W	0
0	Disable XCLK gate	[0] = 0, Enable source driver clock gating [0] = 1, Disable source driver clock gating	R/W	0

11.2.24 Dithering Configuration Registers

11.2.24.1 [0400h] Dithering Configuration Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					Dithering mode select		Dithering start

Bit	Name	Description	R/W	Reset Value
15:3	Reserved	System reserved	R	0000_0000_0000_0
2:1	Dithering mode select	[2:1] / Dithering mode select 00 / 256 gray to 16 gray 01 / 256 gray to 8 gray 10 / 256 gray to 4 gray 11 / 256 gray to 2 gray	R/W	00
0	Dithering start	Dithering start enable.	R/W	0

11.2.24.2 [0402h] Dithering Status Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Dithering status

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_0000
0	Dithering status	[0] = 0, Dithering is done. [0] = 1, Dithering is busy.	R/W	0

11.2.24.3 [040Ah] Dithering Interrupt Raw Status Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Dithering completed interrupt raw

	status

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_000
0	Dithering completed interrupt raw status	[0] = 0, Raw dithering completed interrupt is not occurred. [0] = 1, Raw dithering completed interrupt is occurred.	R/W	0

11.2.24.4 [040Ch] Dithering Interrupt Masked Status Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Dithering completed interrupt masked status

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_000
0	Dithering completed interrupt masked status	[0] = 0: Masked dithering completed interrupt is not occurred. [0] = 1: Dithering completed interrupt is occurred.	R/W	0

11.2.24.5 [040Eh] Dithering Interrupt Enable Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							Dithering completed interrupt enable

Bit	Name	Description	R/W	Reset Value
15:1	Reserved	System reserved	R	0000_0000_0000_000

Bit	Name	Description	R/W	Reset Value
0	Dithering completed interrupt enable	[0] = 0: Disable dithering completed interrupt [0] = 1: Enable dithering completed interrupt	R/W	0

11.2.24.6 [0410h] Dithering Pixel Rectangular X-Start Register

15	14	13	12	11	10	9	8
Reserved				Dithering x-start [11:8]			
7	6	5	4	3	2	1	0
Dithering x-start [7:0]							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	Dithering x-start	X-start for Dithering.	R/W	0000_0000_0000

11.2.24.7 [0412h] Dithering Pixel Rectangular Y-Start Register

15	14	13	12	11	10	9	8
Reserved				Dithering y-start [11:8]			
7	6	5	4	3	2	1	0
Dithering y-start [7:0]							

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	System reserved	R	0000
11:0	Dithering y-start	Y-start for Dithering.	R/W	0000_0000_0000

11.2.24.8 [0414h] Dithering Pixel Rectangular X-End/Horizontal Size Register

15	14	13	12	11	10	9	8
Reserved			Dithering horizontal size				
7	6	5	4	3	2	1	0
Dithering horizontal size							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Dithering x-end/horizontal size	X-end/horizontal size for dithering.	R/W	0_0000_0000_0000

11.2.24.9 [0416h] Dithering Pixel Rectangular Y-End/Vertical Size Register

15	14	13	12	11	10	9	8
Reserved			Dithering y-end/vertical Size				
7	6	5	4	3	2	1	0
Dithering y-end/vertical size							

Bit	Name	Description	R/W	Reset Value
15:13	Reserved	System reserved	R	000
12:0	Dithering y-end/vertical size	Y-end/vertical size for dithering.	R/W	0_0000_ 0000_0000

11.2.24.10 [0420h] Dithering Buffer Start Address Register 0

15	14	13	12	11	10	9	8
Start address of dithering [15:8]							
7	6	5	4	3	2	1	0
Start address of dithering [7:0]							

Bit	Name	Description	R/W	Reset Value
15:0	Start address of dithering [15:0]	Start address [15:0] for dithering	R/W	0000_0000_ 0000_0000

11.2.24.11 [0422h] Dithering Buffer Start Address Register 1

15	14	13	12	11	10	9	8
						Start address of dithering [25:24]	
7	6	5	4	3	2	1	0
Start address of dithering [23:16]							

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	System reserved	R	000
9:0	Start address of dithering [25:16]	Start address [25:16] for dithering	R/W	00_0000_0000

11.2.25 Instruction Parameter Configuration Register

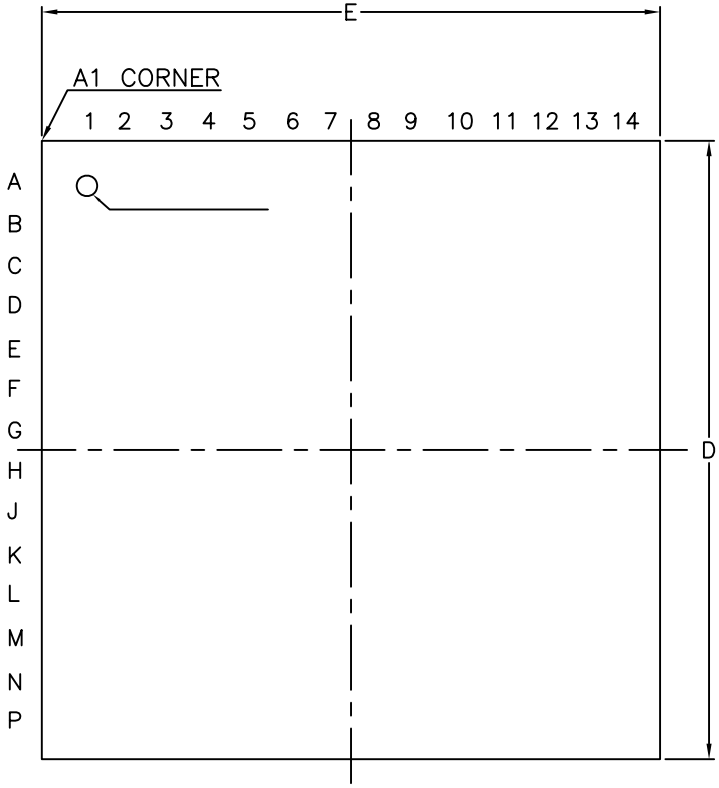
11.2.25.1 [0800h] Instruction Parameter Write Port Register

15	14	13	12	11	10	9	8
Instruction Parameter Write Port							

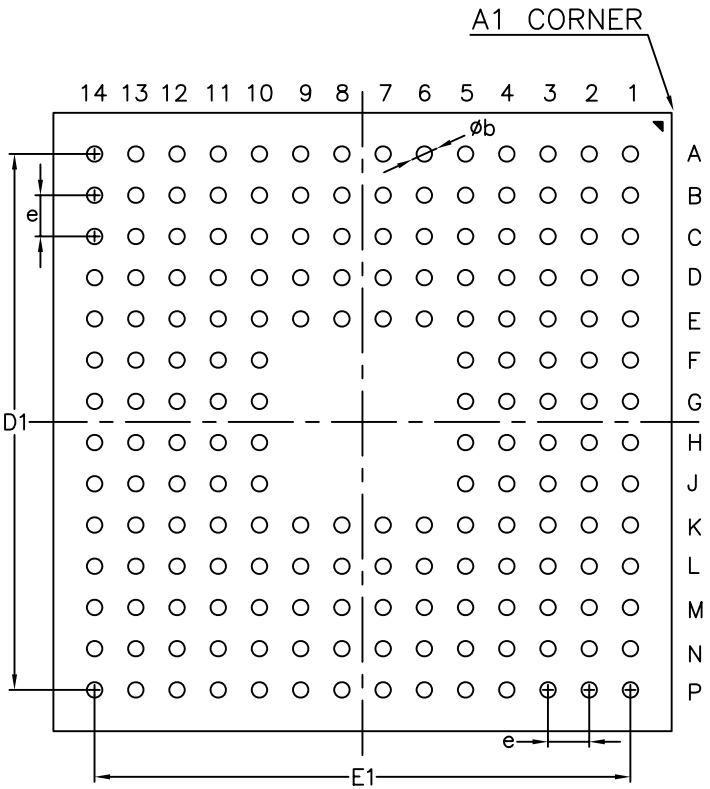
7	6	5	4	3	2	1	0
Instruction Parameter Write Port							

Bit	Name	Description	R/W	Reset Value
15:0	Instruction Parameter Write Port	Instruction Parameter Write Port	W	0000_0000_ 0000_0000

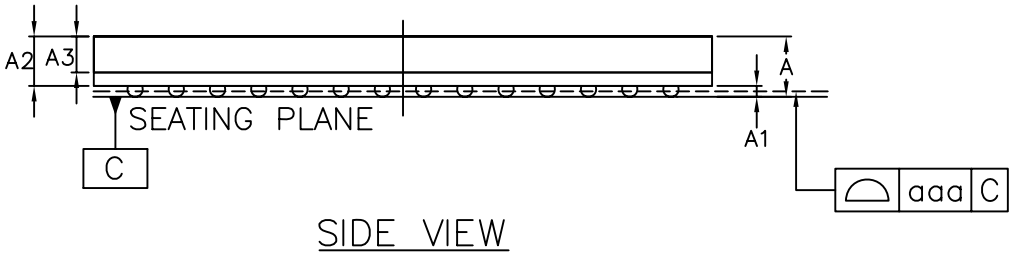
12 Mechanical Data



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.27
A1	0.16	0.21	0.26
A2	0.91	0.96	1.01
A3	0.65	0.70	0.75
b	0.25	0.30	0.35
D	11.90	12.00	12.10
E	11.90	12.00	12.10
D1	10.30	10.40	10.50
E1	10.30	10.40	10.50
e	0.75	0.80	0.85
aaa	0.08 BSC		

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO 275 GGAE–1.