



## 2.13 inch E-paper Display Series



**GDEH0213B73**

Dalian Good Display Co., Ltd.

# Product Specifications



<b>Customer</b>	<b>Standard</b>
<b>Description</b>	<b>2.13" E-PAPER DISPLAY</b>
<b>Model Name</b>	<b>GDEH0213B73</b>
<b>Date</b>	<b>2019/06/13</b>
<b>Revision</b>	<b>2.0</b>

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## Revision History

<b>Rev.</b>	<b>Issued Date</b>	<b>Revised Contents</b>
1.0	June.26.2018	Preliminary
1.1	Dec.07.2018	Increasing the Brand of components
2.0	May.23.2019	Update the reliability test conditions

## 1. General Description

### 1.1 Over View

GDEH0213B73 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.13" active area contains 250×122 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM.LUT, VCOM and border are supplied with each panel.

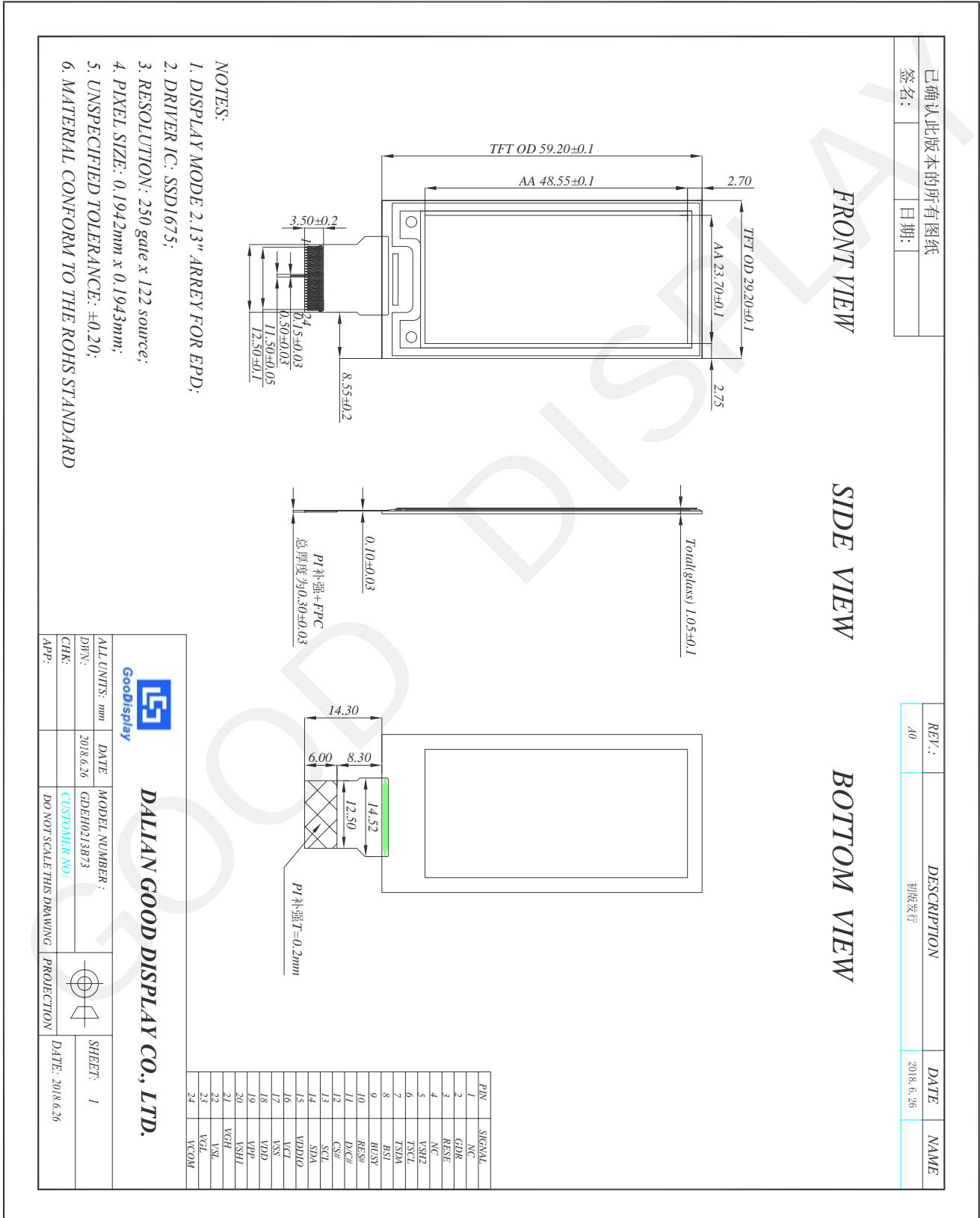
### 1.2 Features

- Support partial refresh
- 250×122 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/built-in temperature sensor

### 1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	122(H)×250(V)	Pixel	Dpi: 130
Active Area	23.7(H)×48.55(V)	mm	
Pixel Pitch	0.1942×0.1943	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.2(H)×59.2 (V) ×1.05(D)	mm	
Weight	3.0±0.2	g	

### 1.4 Mechanical Drawing of EPD module



## 1.5 Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VSH2	This pin is Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS1	Bus selection pin	Note 1.5-5
9	BUSY	Busy state output pin	Note 1.5-4
10	RES #	Reset	Note 1.5-3
11	D/C #	Data /Command control pin	Note 1.5-2
12	CS #	Chip Select input pin	Note 1.5-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	This pin is Positive Source driving voltage	
21	VGH	This pin is Positive Gate driving voltage	
22	VSL	This pin is Negative Source driving voltage	
23	VGL	This pin is Negative Gate driving voltage	
24	VCOM	These pins are VCOM driving voltage	

Note 1.5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.

Note 1.5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 1.5-3: This pin (RES#) is reset signal input. The Reset is active low.

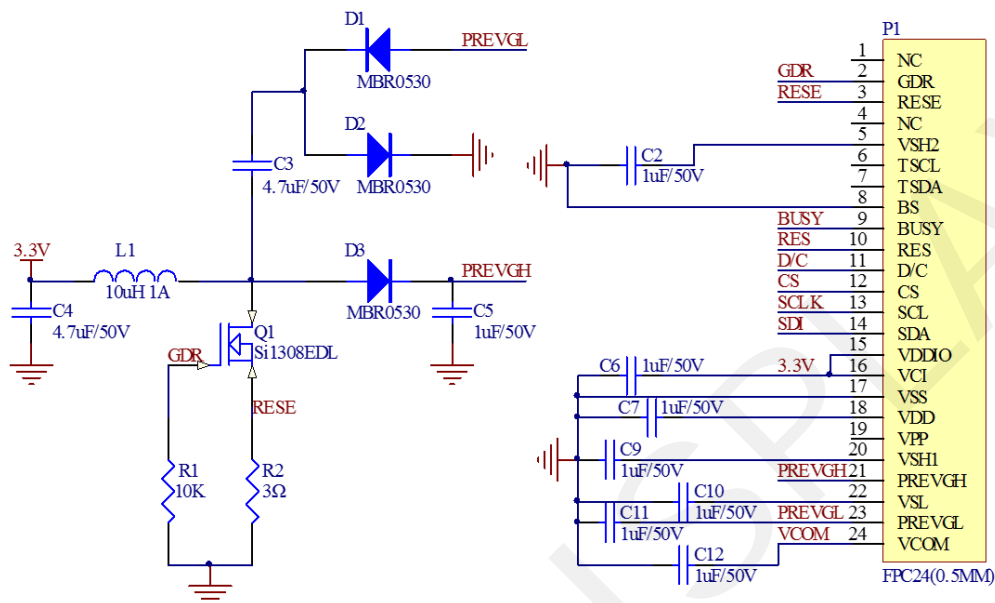
Note 1.5-4: This pin (BUSY) is Busy state output pin. When Busy is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 1.5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected.



### 1.6 Reference Circuit



**Note :**

1. Inductor L1 is wire-wound inductor. There are no special requirements for other parameters.
2. Suggests using Si1304BDL or Si1308EDL TUBE MOS (Q1) , otherwise it may affect the normal boost of the circuit.
3. The default circuit is 4-wire SPI. If the user wants to use 3-wire SPI.
4. Default voltage value of all capacitors is 50V.

## 1.7 Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display `s E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.

DESPI Development Kit consists of the development board and the pinboard.

More details about the Development Kit, please click to the following link:

[http://www.e-paper-display.com/products\\_detail/productId=402.html](http://www.e-paper-display.com/products_detail/productId=402.html)

## 2. Environmental

### 2.1 HANDLING, SAFETY AND ENVIRONMENTAL REQUIREMENTS

<b>WARNING</b>
----------------

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.
--

<b>CAUTION</b>
----------------

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
--

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
---

IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
---

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

<b>Mounting Precautions</b>
-----------------------------

(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
---

(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
---

(3) You should adopt radiation structure to satisfy the temperature specification.
--

(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
--

(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
--

(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
--

(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.
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Product specification	The data sheet contains final product specifications.
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<b>Limiting values</b>
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
<b>Application information</b>
Where application information is given, it is advisory and does not form part of the specification.

<b>Product Environmental certification</b>
ROHS
<b>REMARK</b>
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

## 2.2 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=50°C RH=30%RH, For 240Hr	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T=70°C RH=40%RH For 240Hr Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25°C, for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=40°C, RH=90%RH, For 168Hr	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=60°C, RH=80%RH, For 240Hr Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25°C (30min)~70°C (30min), 100 Cycle Test in white pattern	IEC 60 068-2-14NB	
8	Package Vibration	1.04G, Frequency : 10~500Hz Direction : X,Y,Z Duration: 1hours in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence: 1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
10	UV exposure Resistance	765 W/m <sup>2</sup> for 168hrs, 40°C	IEC 60068-2-5 Sa	
11	Electrostatic discharge	Machine model: +/-250V, 0Ω, 200pF	IEC61000-4-2	

Actual EMC level to be measured on customer application.

Note1: Stay white pattern for storage and non-operation test.

Note2: Operation is black/white/red pattern , hold time is 150S.

Note3: The function, appearance, opticals should meet the requirements of the test before and after the test. Note4 : Keep testing after 2 hours placing at 20°C -25°C.

### 3. Electrical Characteristics

#### 3.1 ABSOLUTE MAXIMUM RATING

Table 3.1-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
VCI	Logic supply voltage	-0.5 to +6.0	V
TOPR	Operation temperature range	0 to 50	°C
TSTG	Storage temperature range	-25 to 60	°C
-	Humidity range	40~70	%RH

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

Note 3-1: Tstg is the transportation condition, the transport time is within 10 days for -25°C ~0°C or 50°C~60°C.

#### 3.2 DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, TOPR=25°C.

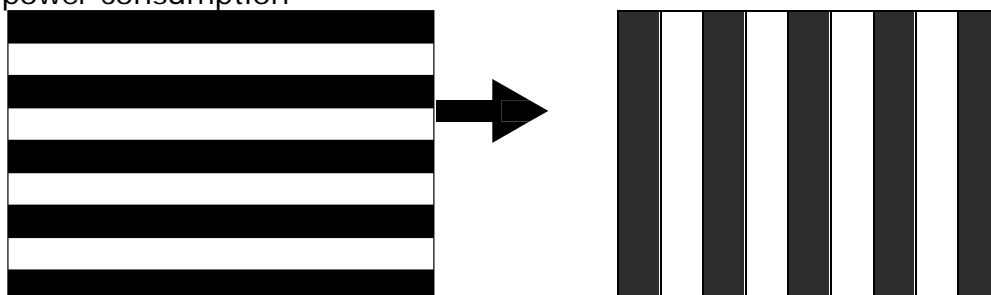
Table 3.2-1: DC Characteristics

Symbol	Parameter	Test	Applicable pin	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	VCI	2.2	3	3.7	V
VIH	High level input	-	SDA, SCL, CS#, D/C#, RES#, BS1	0.8VDDIO	-	-	V
VIL	Low level input voltage	-		-	-	0.2VDDI	V
VOH	High level output	IOH = -100uA	BUSY,	0.9VDDIO	-	-	V
VOL	Low level output	IOL = 100uA		-	-	0.1VDDI	V
Iupdate	Module operating	-	-	-	4.5	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-	-	2	uA

- The Typical power consumption is measured using associated 25°C waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 3-2)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 3-2

The Typical power consumption



### 3.3 Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.2V to 3.7V, TOPR=25°C

#### Write mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

#### Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIG	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

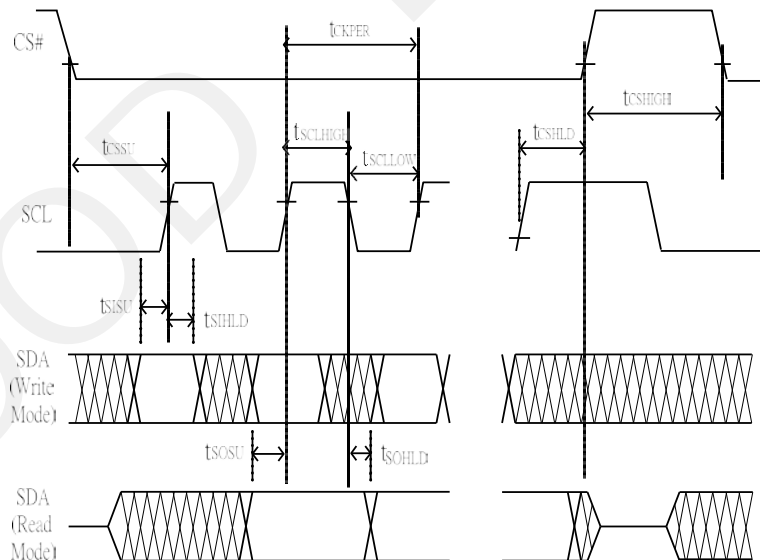


Figure 3.3-1 : Serial peripheral interface characteristics

### 3.4 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	-	18	mAs	-
Deep sleep mode	-	25°C	-	2	uA	-

mAs=update average current×update time

### 3.5 MCU Interface

#### 3.5-1) MCU interface selection

The GDEH0213B73 can support 3-wire/4-wire serial peripheral interface. In the Module, the MCU interface is pin selectable by BS1 pins shown in.

**Table 3.5-1: MCU interface selection**

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) - 9 bits SPI

#### 3.5-2) MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#, The control pins status in 4-wire SPI in writing command/data is shown in Table 7- 2 and the write procedure 4-wire SPI is shown in Figure 7-2.

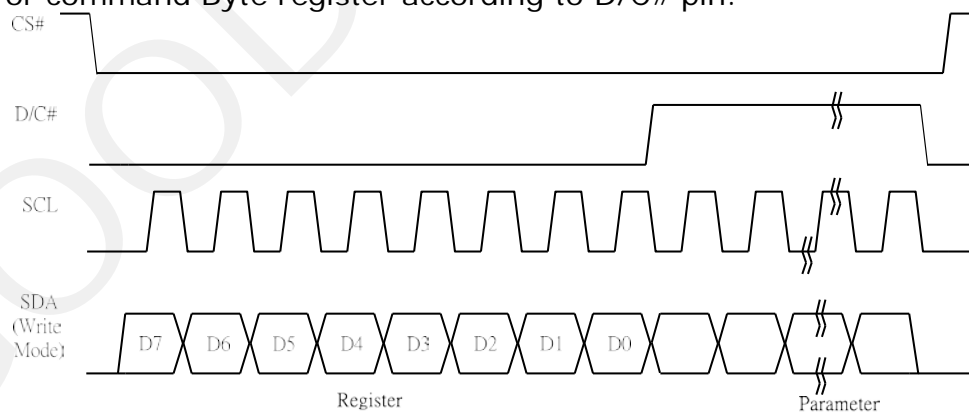
**Table 3.5-2 : Control pins status of 4-wire SPI**

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write	↑	Command bit	L	L
Write data	↑	Data bit	H	L

**Note:**

- (1) L is connected to VSS and H is connected to VDDIO
- (2) ↑ stands for rising edge of signal

In the write mode, SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

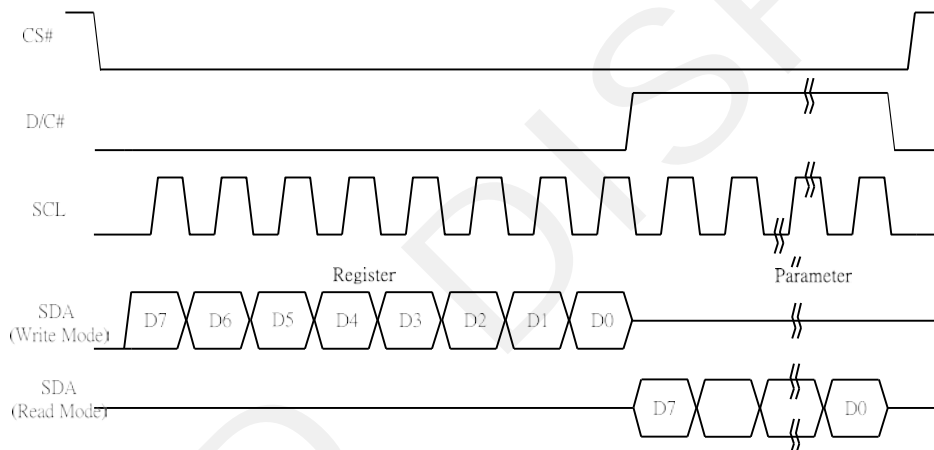


**Figure 3.5-1: Write procedure in 4-wire SPI mode**



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.



**Figure v-2: Read procedure in 4-wire SPI mode**

### 3.5-3) MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.

**Table 3.5-3 : Control pins status of 3-wire SPI**

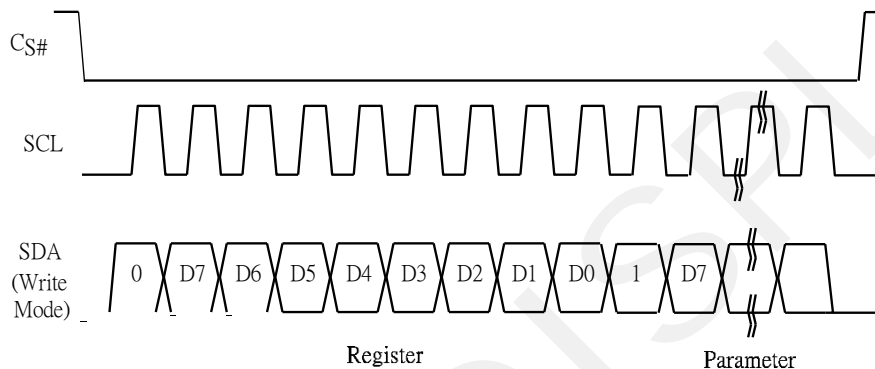
Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

**Note:**

(1)L is connected to VSS and H is connected to VDDIO

(2)↑ stands for rising edge of signal

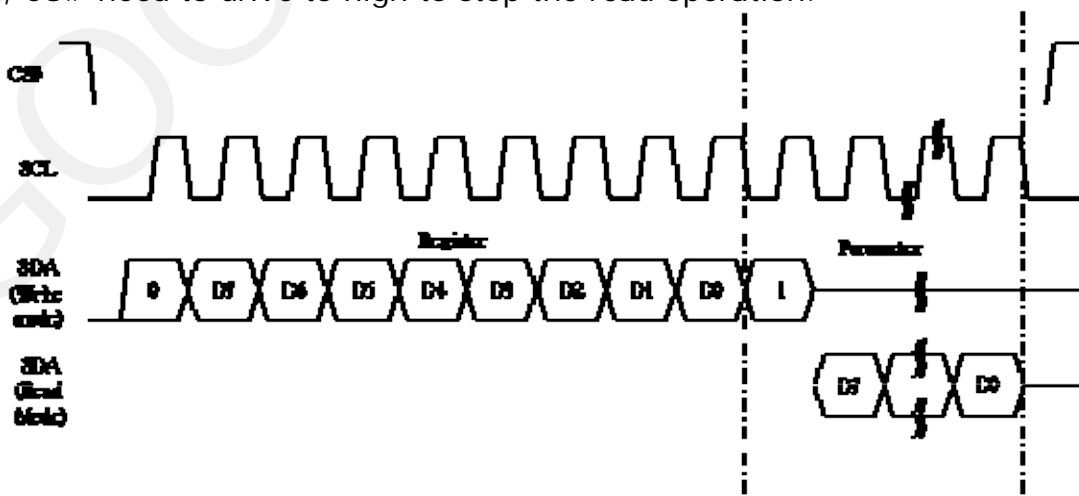
In the write operation, a 9-bit data will be shifted into the shift register on each clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. shows the write procedure in 3-wire SPI



**Figure 3.5-3: Write procedure in 3-wire SPI mode**

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C#=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0.
4. D/C#=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on each falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.



**Figure 3.5-3: Read procedure in 3-wire SPI mode**

### 3.6 Temperature sensor operation

Following is the way of how to sense the ambient temperature of the module. First, use an external temperature sensor to get the temperature value and converted it into HEX format with below mapping table, then send command 0x1A with the HEX temperature value to the module thru the SPI interface.

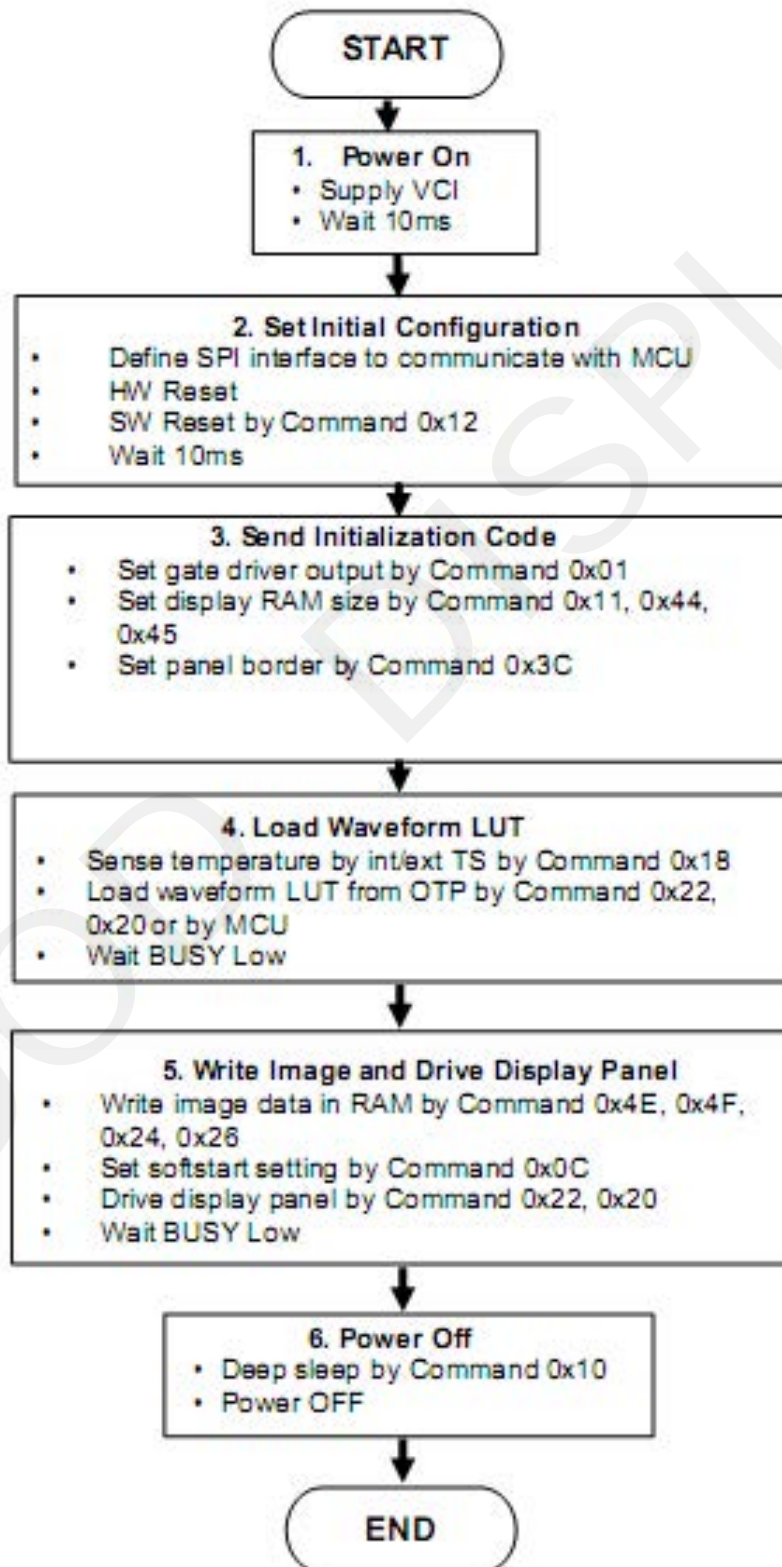
The temperature value to HEX conversion is as follow:

1. If the Temperature value MSByte bit D11 = 0, then  
The temperature is positive and value (DegC) = + (Temperature value) / 16
2. If the Temperature value MSByte bit D11 = 1, then  
The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

## 4. Typical Operating Sequence

### 4.1 Normal Operation Flow



## 5. COMMAND TABLE

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description				
0	0	01	01	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 127h [POR], 296 MUX MUX Gate lines setting as (A[8:0] + 1). B[2:0] = 000 [POR]. Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ... B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...295 (left and right gate interlaced) SM=1, G0, G2, G4 ...G294, G1, G3, ...G295 B[0]: TB TB = 0 [POR], scan from G0 to G295 TB = 1, scan from G295 to G0.				
0	1		A7	A6	A5	A4	A3	A2	A1	A0						
0	1		0	0	0	0	0	0	0	A8						
0	1		0	0	0	0	0	B2	B1	B0						
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 12V to 20V				
0	1		0	0	0	A4	A3	A2	A1	A0						
													A[4:0]	VGH	A[4:0]	VGH
													07h	12	10h	16.5
													08h	12.5	11h	17
													09h	13	12h	17.5
													0Ah	13.5	13h	18
													0Bh	14	14h	18.5
													0Ch	14.5	15h	19
													0Dh	15	16h	19.5
											0Eh	15.5	17h	20		
											0Fh	16	Other	NA		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Driving	
0	1		B7	B6	B5	B4	B3	B2	B1	B0	voltage	
0	1		C7	C6	C5	C4	C3	C2	C1	C0	Control	

A[7]/B[7] = 1,  
VSH1/VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,  
VSH1/VSH2 voltage setting from 9V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7:0]	VSL
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	08	0	0	0	0	1	0	0	0	User Command OTP Program	Program User Command Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	09	0	0	0	0	1	0	0	1	Write Register for User Command	Write Register for User Command Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of User Command Setting
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0A	0	0	0	0	1	0	1	0	Read Register for User Command	Read Register for User Command

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																											
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:																											
0	1		1	A6	A5	A4	A3	A2	A1	A0																													
0	1		1	B6	B5	B4	B3	B2	B1	B0																													
0	1		1	C6	C5	C4	C3	C2	C1	C0																													
0	1		0	0	D5	D4	D3	D2	D1	D0																													
<table border="1"> <thead> <tr> <th>Bit[6:4]</th> <th>Driving Strength Selecti</th> </tr> </thead> <tbody> <tr><td>000</td><td>1 (Weakest)</td></tr> <tr><td>001</td><td>2</td></tr> <tr><td>010</td><td>3</td></tr> <tr><td>011</td><td>4</td></tr> <tr><td>100</td><td>5</td></tr> <tr><td>101</td><td>6</td></tr> <tr><td>110</td><td>7</td></tr> </tbody> </table>												Bit[6:4]	Driving Strength Selecti	000	1 (Weakest)	001	2	010	3	011	4	100	5	101	6	110	7												
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000	1 (Weakest)																																						
001	2																																						
010	3																																						
011	4																																						
100	5																																						
101	6																																						
110	7																																						
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Bit[3:0]	Min Off Time Setting of GDR [ Time unit ]																																						
0000-0011	NA																																						
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0111	4.6																																						
1000	5.4																																						
1001	6.3																																						
1010	7.3																																						
1011	8.4																																						
1100	9.8																																						
1101	11.5																																						
1110	13.8																																						
1111	16.5																																						
D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1																																							
<table border="1"> <thead> <tr> <th>Bit[1:0]</th> <th>Duration of Phase [Approximation]</th> </tr> </thead> <tbody> <tr><td>00</td><td>10ms</td></tr> <tr><td>01</td><td>20ms</td></tr> <tr><td>10</td><td>30ms</td></tr> <tr><td>11</td><td>40ms</td></tr> </tbody> </table>												Bit[1:0]	Duration of Phase [Approximation]	00	10ms	01	20ms	10	30ms	11	40ms																		
Bit[1:0]	Duration of Phase [Approximation]																																						
00	10ms																																						
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10	30ms																																						
11	40ms																																						



R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 295. A[8:0] = 000h [POR] When TB=0: SCN [8:0] = A[8:0] When TB=1: SCN [8:0] = 295 - A[8:0]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2  After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	A1	A0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 -Y decrement, X decrement, 01 -Y decrement, X increment, 10 -Y increment, X decrement, 11 -Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A2	A1	A0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description														
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).														
0	1		0	A6	A5	A4	A3	A2	A1	A0			A[6:4]=n for CD time: 10ms x n A[2:0]=m for Loop time m+1 The max HV ready duration is (10ms x A[6:4]) x (m+1) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.													
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A[2:0]</th> <th>VCI level</th> </tr> </thead> <tbody> <tr> <td>011</td> <td>2.2V</td> </tr> <tr> <td>100</td> <td>2.3V</td> </tr> <tr> <td>101</td> <td>2.4V</td> </tr> <tr> <td>110</td> <td>2.5V</td> </tr> <tr> <td>111</td> <td>2.6V</td> </tr> <tr> <td>Other</td> <td>NA</td> </tr> </tbody> </table> The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).	A[2:0]	VCI level	011	2.2V	100	2.3V	101	2.4V	110	2.5V	111	2.6V	Other	NA
A[2:0]	VCI level																									
011	2.2V																									
100	2.3V																									
101	2.4V																									
110	2.5V																									
111	2.6V																									
Other	NA																									
0	1		0	0	0	0	0	A2	A1	A0																
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature														
0	1		A7	A6	A5	A4	A3	A2	A1	A0																
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. Write to temperature register. [POR]														
0	1		A11	A10	A9	A8	A7	A6	A5	A4																
0	1		A3	A2	A1	A0	0	0	0	0																
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.														
0	1		A11	A10	A9	A8	A7	A6	A5	A4																
0	1		A3	A2	A1	A0	0	0	0	0																

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature SensorControl (WriteCommand to Externaltemperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
											00 Address + pointer	
											01 Address + pointer	
											10 Address + pointer + 1st parameter +2nd pointer	
											11 AddressA[5:0] –Pointer	
											A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.	
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[7:4] Red RAM option
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
											0000 Normal	
											0100 Bypass RAM content as 0	
											1000 Inverse RAM content	
											A[3:0] BW RAM option	
											0000 Normal	
											0100 Bypass RAM content as 0	
											1000 Inverse RAM content	

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Display Update Sequence Option: A[7:0]= FFh (POR)
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
												Enable Clock Signal, Then Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC
												Parameter (in C7)
												Enable Clock Signal, Then Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC
												CF
												Enable Clock Signal, Then Load LUT with DISPLAY Mode 1
												90
												Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1
												BO
												Enable Clock Signal, Then Load LUT with DISPLAY Mode 2
												98
												Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2
												B8
												Enable Clock Signal, Then Load LUT with DISPLAY Mode 1 To
												91
												Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal
												B1
												Enable Clock Signal, Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal
												99
												Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal
												B9
												Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC
												47
												Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC
												4F
												To Enable Clock Signal (CLKEN=1)
												80
												To Enable Clock Signal, then Enable ANALOG (CLKEN=1, ANALOGEN=1)
												CO
												Enable ANALOG Then DISPLAY with DISPLAY Mode 1
												44
												Enable ANALOG Then DISPLAY with DISPLAY Mode 2
												4C
												To DISPLAY with DISPLAY Mode 1
												4
												To DISPLAY with DISPLAY Mode 2
												0C
												To Disable ANALOG, then Disable Clock Signal (CLKEN=0, ANALOGEN=0)
												3
												To Disable Clock Signal (CLKEN=0)
												1

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register. The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 09h [POR], duration = 10s. VCOM sense duration = (A[3:0] + 1) sec
0	1		0	1	0	0	A3	A2	A1	A0		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description				
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.				
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.				
0	1		0	0	0	0	0	1	0	0						
0	1		0	1	1	0	0	0	1	1						
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]				
0	1		A7	A6	A5	A4	A3	A2	A1	A0			A[7:0]	VCOM	A[7:0]	VCOM
													08h	-0.2	44h	-1.7
													0Ch	-0.3	48h	-1.8
													10h	-0.4	4Ch	-1.9
													14h	-0.5	50h	-2
													18h	-0.6	54h	-2.1
													1Ch	-0.7	58h	-2.2
													20h	-0.8	5Ch	-2.3
													24h	-0.9	60h	-2.4
													28h	-1	64h	-2.5
													2Ch	-1.1	68h	-2.6
													30h	-1.2	6Ch	-2.7
													34h	-1.3	70h	-2.8
													38h	-1.4	74h	-2.9
													3Ch	-1.5	78h	-3
											40h	-1.6	Other	NA		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~F[7:0]: Display Mode (Command 0x37, Byte B to Byte G) [5 bytes] G[7:0]~H[7:0]: Waveform Version (Command 0x37, Byte H to Byte K) [4 bytes]				
1	1		A7	A6	A5	A4	A3	A2	A1	A0						
1	1		B7	B6	B5	B4	B3	B2	B1	B0						
1	1		C7	C6	C5	C4	C3	C2	C1	C0						
1	1		D7	D6	D5	D4	D3	D2	D1	D0						
1	1		E7	E6	E5	E4	E3	E2	E1	E0						
1	1		F7	F6	F5	F4	F3	F2	F1	F0						
1	1		G7	G6	G5	G4	G3	G2	G1	G0						
1	1		H7	H6	H5	H4	H3	H2	H1	H0						
1	1		I7	I6	I5	I4	I3	I2	I1	I0						
1	1		J7	J6	J5	J4	J3	J2	J1	J0						
1	1		K7	K6	K5	K4	K3	K2	K1	K0						

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]–J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A5	A4	0	A2	A1	A0		
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [100 bytes], which contains the content of VS [nX-LUT], TP #[nX], RP#[n]. Refer to Session 6.7 Waveform
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	.	.	.	.	.	.	.		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command for OTP content validation. For details, please refer to SSD1675B application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status	CRC Status Read
1	1		A15	A14	A13	A12	A11	A10	A9	A8	Read	A[15:0] is the CRC read out value
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	1	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 [POR] 1: Display Mode2 F[6]: PingPong for Display Mode 2 0: RAM ping-pong disable [POR] 1: RAM ping-pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM ping-pong function is not support for Display Mode 1
0	1		B7	B6	B5	B4	B3	B2	B1	B0	Display Option	
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	1		E7	E6	E5	E4	E3	E2	E1	E0		
0	1		F7	F6	F5	F4	F3	F2	F1	F0		
0	1		G7	G6	G5	G4	G3	G2	G1	G0		
0	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	1		I7	I6	I5	I4	I3	I2	I1	I0		
0	1		J7	J6	J5	J4	J3	J2	J1	J0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	
0	1		A7	A6	A5	A4	A3	A2	A1	A0	for User ID	
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	1		E7	E6	E5	E4	E3	E2	E1	E0		
0	1		F7	F6	F5	F4	F3	F2	F1	F0		
0	1		G7	G6	G5	G4	G3	G2	G1	G0		
0	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	1		I7	I6	I5	I4	I3	I2	I1	I0		
0	1		J7	J6	J5	J4	J3	J2	J1	J0		



R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode OTP program mode A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY
0	1		0	0	0	0	0	0	0	0		
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period A[6:0] = 30h [POR] A[6:0]: Number of dummy line period in term of TGate Available setting 0 to 127.
0	1		0	A6	A5	A4	A3	A2	A1	A0		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set Gate line width (TGate) A[3:0] = 1010 [POR] Remark: Default value will give 50Hz Frame frequency under 48 dummy line pulse setting.
0	1		0	0	0	0	A3	A2	A1	A0		
Frame Frequency [Hz]			Parameter of 0x3A			Parameter of 0x3B						
25			0x29			0x0E						
30			0x46			0x0D						
35			0x48			0x0D						
40			0x48			0x0C						
45			0x28			0x0C						
50			0x0F			0x0C						
55			0x37			0x0B						
60			0x21			0x0B						
65			0x0E			0x0B						
70			0x22			0x0A						
75			0x11			0x0A						
80			0x03			0x0A						
85			0x17			0x09						
90			0x0A			0x09						
95			0x26			0x08						
100			0x1A			0x08						
105			0x0E			0x08						
110			0x04			0x08						
115			0x1D			0x07						
120			0x13			0x07						
125			0x0A			0x07						
130			0x01			0x06						
135			0x22			0x06						
145			0x11			0x06						
150			0x0A			0x06						
155			0x03			0x06						
160			0x1C			0x05						
165			0x15			0x05						
170			0x0E			0x05						
175			0x07			0x05						
180			0x01			0x05						
185			0x21			0x04						
190			0x1B			0x04						
195			0x15			0x04						
200			0x0F			0x04						
Remark: Frame rate setting depends on resolution.												

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border	Select border waveform for VBD
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Waveform Control	A[7:0] = C0h [POR], set VBD as HiZ. A [7:6] :Select VBD option
												A[7:6] Select VBD as
												00 GS Transition,Defined in A[1:0]
												01 Fix Level,Defined in A[5:4]
												10 VCOM
												11[POR] HiZ
												A [5:4] Fix Level Setting for VBD
												A[5:4] VBD level
												00[POR] VSS
												01 VSH1
												10 VSL
												11 VSH2
												A [1:0] GS Transition setting for VBD
												A[1:0] VBD Transition
												00[POR] LUT0
												01 LUT1
												10 LUT2
												11 LUT3
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option
0	1		0	0	0	0	0	0	0	A0	Option	A[0]= 0 [POR] 0 : Read RAM corresponding to 24h 1 : Read RAM corresponding to 26h
										0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start /	Specify the start/end positions of the window address in the X direction by an address unit for RAM
0	1		0	0	A5	A4	A3	A2	A1	A0	End position	A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 13h
0	1		0	0	B5	B4	B3	B2	B1	B0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start /	Specify the start/end positions of the window address in the Y direction by an address unit for RAM
0	1		A7	A6	A5	A4	A3	A2	A1	A0	End position	A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h
0	1		0	0	0	0	0	0	0	A8		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		0	0	0	0	0	0	0	B8		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	46	1	0	0	0	0	1	1	0	Auto Write RED RAM	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Auto Write RED RAM	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate
			A[6:4]		Height		A[6:4]		Height			
			000		8		100		128			
			001		16		101		256			
			010		32		110		296			
			011		64		111		NA			
			A[2:0]		Step Width, POR= 000		A[2:0]		Step Width, POR= 000			
			A[2:0]		Width		A[2:0]		Width			
			000		8		100		128			
			001		16		101		160			
			010		32		110		NA			
			011		64		111		NA			
			BUSY pad will output high during operation.									
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Hieght, POR= 000 Step of alter RAM in Y-direction according to Gate
			A[6:4]		Height		A[6:4]		Height			
			000		8		100		128			
			001		16		101		256			
			010		32		110		296			
			011		64		111		NA			
			A[2:0]		Step Width, POR= 000		A[2:0]		Step Width, POR= 000			
			A[2:0]		Width		A[2:0]		Width			
			000		8		100		128			
			001		16		101		160			
			010		32		110		NA			
			011		64		111		NA			
			During operation, BUSY pad will output high.									

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address X address	Make initial settings for the RAM X address in the address counter (AC)
0	1		0	0	A5	A4	A3	A2	A1	A0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	0	74	0	1	1	1	0	1	0	0	Set Analog Block Control	A[7:0]: 54h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	7E	0	1	1	1	1	1	1	0	Set Digital Block Control	A[7:0]: 3Bh [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

## 6. Optical characteristics

### 6.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 6-1
Gn	2Grey Level	-	-	$DS + (WS - DS) \times n(m-1)$	-	L*	-
CR	Contrast Ratio	indoor	-	10	-	-	-
Panel's life	-	0°C~30°C		5years	-	-	Note 6-2

M: 2

WS : White state, DS : Dark state

Note 16-1 : Luminance meter : Eye - One Pro Spectrophotometer ;

Note 16-2: We guarantee display quality from 0°C~30°C generally, If operation ambient temperature from 0~50°C, will Offer special waveform by Good Display.

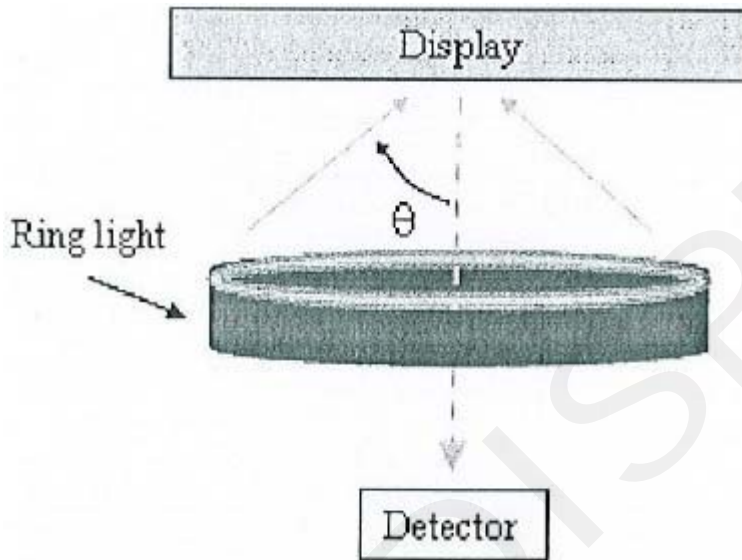
We don't guarantee 5 years pixels display quality for humidity below 45%RH or above 70%RH;

Suggest Updated once a day;

### 6.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) :

R1: white reflectance                      Rd: dark reflectance  
 CR = R1/Rd

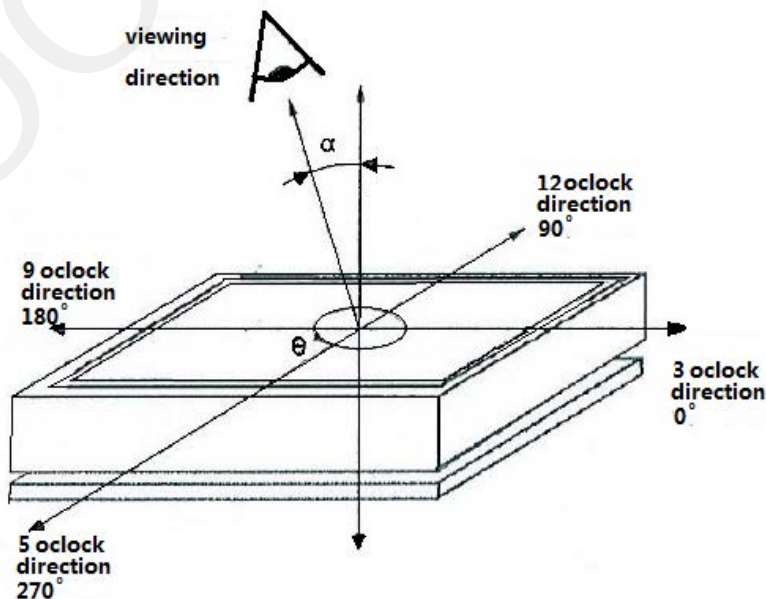


### 6.3 Reflection Ratio

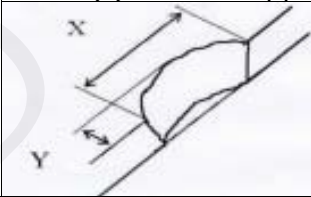
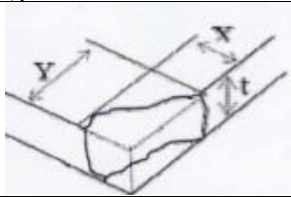
The reflection ratio is expressed as :

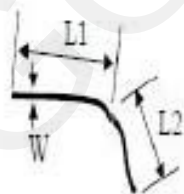
$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

$L_{\text{center}}$  is the luminance measured at center in a white area ( $R=G=B=1$ ) .  $L_{\text{white board}}$  is the luminance of a standard white board . Both are measured with equivalent illumination source . The viewing angle shall be no more than 2 degrees .



### 7. Point and line standard

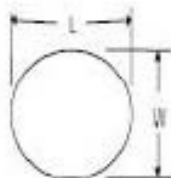
Shipment Inspection Standard						
Equipment: Electrical test fixture, Point gauge						
Outline dimension	29.2(H)×59.2 (V) ×1.05(D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature 19°C~25°C	Humidity 55%±5%RH	Illuminance 800~1300Lux	Distance 300 mm	Time 35Sec	Angle
Defet type	Inspection method	Standard		Part-A	Part-B	
Spot	Electric Display	D≤0.25 mm		Ignore	Ignore	
		0.25 mm<D≤0.4 mm		N≤4	Ignore	
		D>0.4 mm		Not Allow	Ignore	
Display unwork	Electric Display	Not Allow		Not Allow	Ignore	
Display error	Electric Display	Not Allow		Not Allow	Ignore	
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm, W≤0.2 mm		Ignore	Ignore	
		2.0mm<L≤5.0mm, 0.2<W≤0.3mm,		N≤2	Ignore	
		L>5 mm, W>0.3 mm		Not Allow	Ignore	
PS Bubble	Visual/Film card	D≤0.2mm		Ignore	Ignore	
		0.2mm≤D≤0.35mm & N≤4		N≤4	Ignore	
		D>0.35 mm		Not Allow	Ignore	
Corner /Edge chipping	Visual/Film card	X≤6mm, Y≤0.4mm, Do not affect the electrode circuit (Edge chipping)				
		X≤1mm, Y≤1mm, Do not affect the electrode circuit( (Corner chipping) Ignore				
						
Remark	1. Cannot be defect & failure cause by appearance defect;					
	2. Cannot be larger size cause by appearance defect;					
	L=long		W=wide		D=point size N=Defects NO	



$L = L1 + L2$

Line Defect

L=long

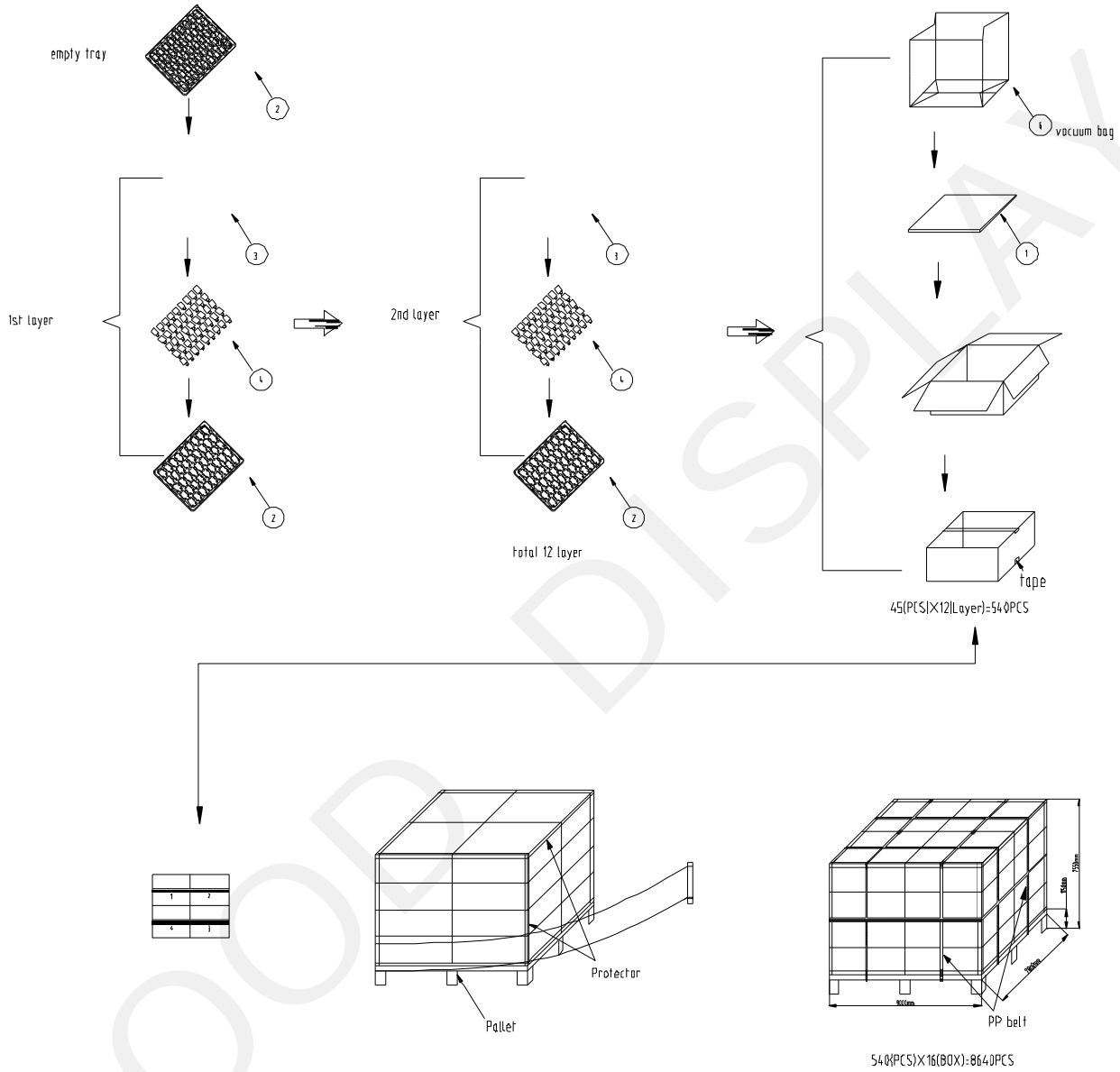


$D = (L+W)/2$

Spot Defect

W=wide D=pointsize

## 8. Packing





## 9. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.